DRV8304 38-V 3-Phase Smart Gate Driver

1 Features

- 6-V to 38-V, Triple Half-Bridge Gate Driver With Integrated 3x Current Sense Amplifiers (CSA)
  - 40-V Absolute Maximum Rating
  - Fully Optimized for 12-V and 24-V DC Rails
  - Drives High-Side and Low-Side N-Channel MOSFETs
  - Supports 100% PWM Duty Cycle
- Smart Gate-Drive Architecture
  - Adjustable Slew-Rate Control for Better EMI and EMC Performance
  - V_{GS} Hand-Shake and Minimum Dead-Time Insertion to Avoid Shoot-Through
  - 15-mA to 150-mA Peak Source Current
  - 30-mA to 300-mA Peak Sink Current
- 6x, 3x, 1x and Independent PWM Modes
  - Supports 120º Sensored Operation
- Integrated Gate-Driver Power Supplies
  - High-Side Doubler Charge Pump
  - Low-Side Linear Regulator
- Integrated Triple Current-Shunt Amplifiers
  - Adjustable Gain (5, 10, 20, 40 V/V)
  - Bidirectional or Unidirectional Support
- SPI or Hardware Device Variants
- Supports 1.8-V, 3.3-V, and 5-V Logic Inputs
- Low-Power Sleep Mode
- Linear Voltage Regulator, 3.3-V, 30-mA
- Integrated Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - MOSFET V_{DS} Overcurrent Protection (OCP)
  - MOSFET Shoot-Through Protection
  - Gate Driver Fault (GDF)
  - Thermal Warning and Shutdown (OTW/OTSD)
  - Fault Condition Indicator (nFAULT)

2 Applications

- Printers
- BLDC Motor Modules
- White Goods
- CPAPs, Fans, and Pumps
- Drones, Robotics, and RC Toys
- ATM and Currency Counting

3 Description

The DRV8304 device is an integrated gate driver for 3-phase brushless DC (BLDC) motors applications for 12-V and 24-V DC rails. These applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal current control of BLDC motors. The device integrates three current-sense amplifiers (CSA) for sensing the phase currents of BLDC motors for optimum FOC and current-control system implementation. An AUTOCAL feature automatically calibrates the CSA offset error for accurate current sensing.

The device is based on smart gate-drive (SGD) architecture to eliminate the need of any external gate components (resistors and Zener diodes) while fully protecting the external FETs. The SGD architecture optimizes dead time to avoid any shoot-through conditions, provides flexibility in decreasing electromagnetic interference (EMI) by gate slew-rate control, and protects against any gate-short conditions through V_{GS} hand-shaking and dead time insertion. Strong pulldown current also prevents any dv/dt gate turnon.

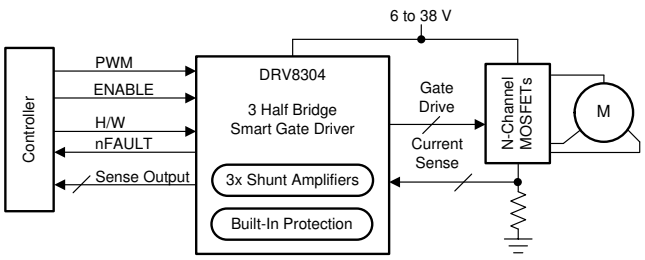
Various PWM control modes (1x, 3x, 6x, and independent) are supported for simple interfacing to control circuits that can be powered by the 30-mA, 3.3-V internal regulator. These modes decrease the number of output peripherals of the controller for the specific motor-control requirements and provide flexibility of control. The device also has a 1x mode for sensored trapezoidal control of the BLDC motor by using the internal block-commutation table. The device can also be configured to drive multiple loads, such as solenoids, in independent mode.

Device Information(1)

PART NUMBER	PACKAGE	INTERFACE
DRV8304	VQFN (40)	Hardware
		SPI

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2018) to Revision B **Page**

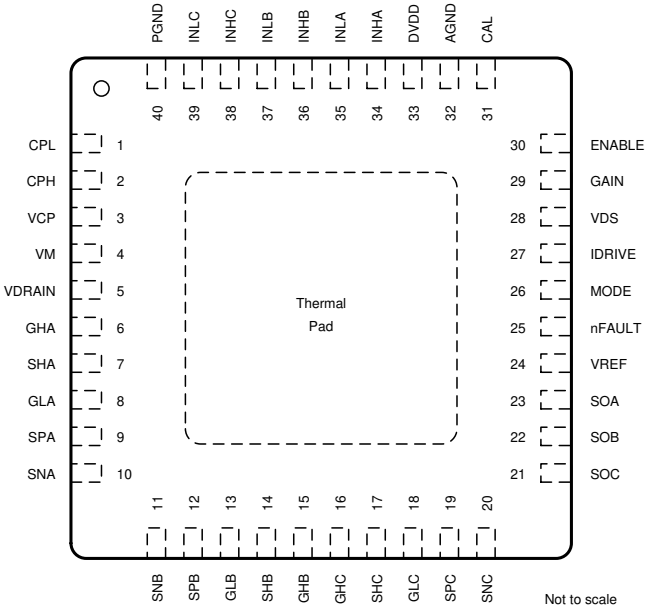
- Deleted preview status from the SPI version of the device ... 1

Changes from Original (November 2017) to Revision A **Page**

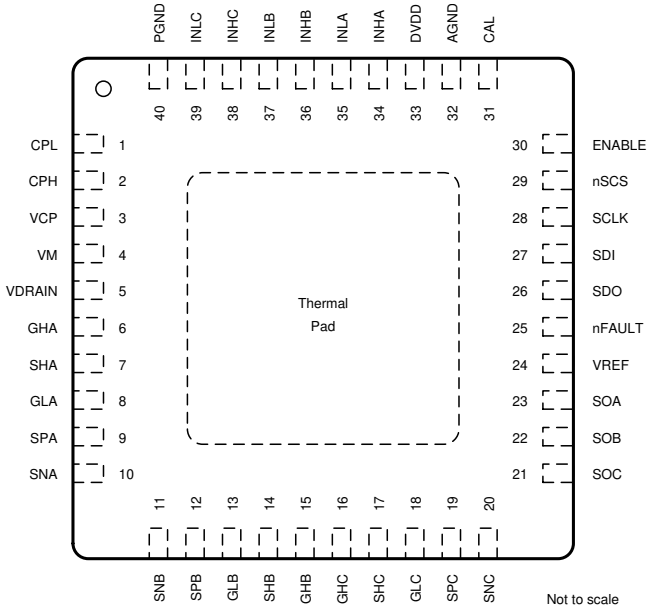
- Changed the data sheet from *Advance Information* to *Production Data* ... 1

5 Pin Configuration and Functions

DRV8304H RHA Package
40-Pin VQFN With Exposed Thermal Pad
Top View



DRV8304S RHA Package
40-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8304H	DRV8304S		
AGND	32	32	PWR	Device analog ground. Connect to system ground.
CAL	31	31	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform offset calibration.
CPH	2	2	PWR	Charge pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
CPL	1	1	PWR	Charge pump switching node. Connect a X5R or X7R, 22-nF, VM-rated ceramic capacitor between the CPH and CPL pins.
DVDD	33	33	PWR	3.3-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	30	30	I	Gate driver enable. When this pin is logic low the device enters a low power sleep mode. An 5 to 32-µs low pulse can be used to reset fault conditions.
GAIN	29	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	6	6	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	16	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	8	8	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	13	13	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	18	18	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	27	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	34	34	I	High-side gate driver control input. This pin controls the output of the high-side gate driver (GHA).

(1) PWR = power, I = input, O = output, OD = open-drain

Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8304H	DRV8304S		
INHB	36	36	I	High-side gate driver control input. This pin controls the output of the high-side gate driver (GHB).
INHC	38	38	I	High-side gate driver control input. This pin controls the output of the high-side gate driver (GHC).
INLA	35	35	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver (GLA).
INLB	37	37	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver (GLB).
INLC	39	39	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver (GLC).
MODE	26	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
nFAULT	25	25	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pullup resistor.
nSCS	—	29	I	Serial chip select. A logic low on this pin enables serial interface communication.
PGND	40	40	PWR	Device power ground. Connect to system ground.
SCLK	—	28	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	27	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	26	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor.
SHA	7	7	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHB	14	14	I	High-side source sense input. Connect to the high-side power MOSFET source.
SHC	17	17	I	High-side source sense input. Connect to the high-side power MOSFET source.
SNA	10	10	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNB	11	11	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SNC	20	20	I	Shunt amplifier input. Connect to the low-side of the current shunt resistor.
SOA	23	23	O	Shunt amplifier output.
SOB	22	22	O	Shunt amplifier output.
SOC	21	21	O	Shunt amplifier output.
SPA	9	9	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPB	12	12	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPC	19	19	I	Low-side source sense and shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
VCP	3	3	PWR	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VCP and VM pins.
VDRAIN	5	5	I	High-side MOSFET drain sense input. Connect to the common point of the external MOSFET drains.
VDS	28	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	4	4	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1-µF, VM-rated ceramic and greater than or equal to 10-uF local capacitance between the VM and PGND pins.
VREF	24	24	PWR	Shunt amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	40	V
Voltage differential between any ground pin (AGND, DGND, PGND)	–0.5	0.5	V
Internal logic regulator voltage (DVDD)	–0.3	3.8	V
MOSFET voltage sense (VDRAIN)	–0.3	40	V
Charge pump voltage (VCP, CPH)	–0.3	VM + 13.5	V
Charge pump negative switching pin voltage (CPL)	–0.3	VM	V
Digital pin voltage (SCLK, SDI, nSCS, ENABLE, VDS, IDRIVE, MODE, GAIN, CAL INHX, INLX)	–0.3	5.75	V
Open drain output current range (nFAULT, SDO)	0	5	mA
Continuous high-side gate pin voltage (GHX)	–2	VCP + 0.5	V
Pulsed 200 ns high-side gate pin voltage (GHX)	–5	VCP + 0.5	V
High-side gate voltage with respect to SHX (GHX)	–0.3	13.5	V
Continuous phase node pin voltage (SHX)	–2	VM + 2	V
Pulsed 200 ns phase node pin voltage (SHX)	–5	VM + 2	V
Continuous low-side gate pin voltage (GLX)	–1	13.5	V
Pulsed 200 ns low-side gate pin voltage (GLX)	–5	13.5	V
Gate pin source current (GHX, GLX)	Internally limited		A
Gate pin sink current (GHX, GLX)	Internally limited		A
Continuous shunt amplifier input pin voltage (SPX, SNX)	–1	1	V
Pulsed 200 ns shunt amplifier input pin voltage (SPX, SNX)	–2	2	V
Reference pin input voltage (VREF)	–0.3	5.75	V
Shunt amplifier output pin voltage range (SOX)	–0.3	VREF	V
Shunt amplifier output pin current range (SOX)	0	5	mA
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Power supply voltage range	6	38	V
V_I	Logic level input voltage range	0	5.5	V

Recommended Operating Conditions (continued)

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
f_{PWM}	Applied PWM signal (INHX, INLX)		200 (1)	kHz
I_{GATE_HS}	High-side average gate drive current (GHX)		15 (1)	mA
I_{GATE_LS}	Low-side average gate drive current (GLX)		15 (1)	mA
I_{DVDD}	DVDD external load current		30 (1)	mA
I_{SO}	Shunt amplifier output current loading (SOX)	0	5	mA
V_{OD}	Open drain pull up voltage (nFAULT, SDO)	0	5.5	V
I_{OD}	Open drain output current (nFAULT, SDO)	0	5	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8304 RHA (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VM)						
I_{VM}	VM operating supply current	ENABLE = 1; INH_X = 0 V; INL_X = 0 V		5	7	mA
I_{VMQ}	VM sleep mode supply current	ENABLE = 0; V_{VM} = 24 V; T_A = 25°C		20	40	µA
		ENABLE = 0, V_{VM} = 24 V, T_A = 125°C (1)			100	µA
t_{RST}	Reset pulse time	ENABLE = 0 V period to reset faults	15		40	µs
t_{SLEEP}	Sleep time	ENABLE = 0 V to driver tri-stated			200	µs
t_{WAKE}	Wake-up time	V_{VM} > V_{UVLO}; ENABLE = 3.3 V to output transition			1	ms
V_{DVDD}	Internal logic regulator voltage	I_{DVDD} = 0 to 30 mA	2.9	3.3	3.6	V
CHARGE PUMP (CPH, CPL, VCP)						
V_{VCP}	VCP operating voltage with respect to VM	V_M = 12 to 38 V; I_{VCP} = 0 to 15 mA	7	10	11.5	V
		V_M = 10 V; I_{VCP} = 0 to 10 mA	6.5	7.5	9.5	V
		V_M = 8 V; I_{VCP} = 0 to 5 mA	5	6	7.5	V
		V_M = 6 V; I_{VCP} = 0 to 1 mA	3.8	4.3	6.5	V
LOGIC-LEVEL INPUTS (CAL, INHX, INLX, SCLK, SDI, nSCS)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V			100	µA

(1) Specified by design and characterization data

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Pulldown Resistance to AGND (CAL, INHX, INLX, SCLK, SDI, nSCS)			100		kΩ
LOGIC-LEVEL INPUTS (ENABLE)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–10		10	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	-5		5	µA
FOUR-LEVEL INPUTS (GAIN, MODE)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	45 kΩ ± 5% to AGND		1.2		V
V_{I3}	Input mode 3 voltage	Hi-Z		2		V
V_{I4}	Input mode 4 voltage	Tied to DVDD		3.3		V
SEVEN-LEVEL INPUTS (IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	18 kΩ ± 5% to AGND		0.5		V
V_{I3}	Input mode 3 voltage	75 kΩ ± 5% to AGND		1.1		V
V_{I4}	Input mode 4 voltage	Hi-Z		1.65		V
V_{I5}	Input mode 5 voltage	75 kΩ ± 5% to DVDD		2.2		V
V_{I6}	Input mode 6 voltage	18 kΩ ± 5% to DVDD		2.8		V
V_{I7}	Input mode 7 voltage	Tied to DVDD		3.3		V
OPEN-DRAIN OUTPUTS (nFAULT, SDO)						
V_{OL}	Output logic low voltage	I_{OD} = 2 mA			0.1	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	–1		1	µA
GATE DRIVERS (GHX, GLX, SHX)						
V_{GHS} (1)	High-side V_{GS} gate drive (gate-to-source)	V_{VM} = 12 to 38 V; I_{HS_GATE} = 0 to 15 mA	7	10	11.5	V
		V_{VM} = 10 V; I_{HS_GATE} = 0 to 10 mA	6.5	7.5	8.5	
		V_{VM} = 8 V; I_{HS_GATE} = 0 to 5 mA	5	6	7	
		V_{VM} = 6 V; I_{HS_GATE} = 0 to 1 mA	3.8	4.3	6.5	
V_{GSL} (1)	Low-side V_{GS} gate drive (gate-to-source)	V_{VM} = 12 to 38 V; I_{LS_GATE} = 0 to 15 mA	7.5	10	12.5	V
		V_{VM} = 10 V; I_{LS_GATE} = 0 to 10 mA	5.5	7.5	9.5	
		V_{VM} = 8 V; I_{LS_GATE} = 0 to 5 mA	3.5	6	8.5	
		V_{VM} = 6 V; I_{LS_GATE} = 0 to 1 mA	3	4.3	6.5	
t_{DEAD}	Output dead time (SPI Device)	DEAD_TIME = 00b		40		ns
		DEAD_TIME = 01b		120		
		DEAD_TIME = 10b		200		
		DEAD_TIME = 11b		400		
t_{DEAD}	Output dead time (HW Device)			120		ns
t_{DRIVE}	Peak gate drive time (SPI Device)	TDRIVE = 00b		500		ns
		TDRIVE = 01b		1000		
		TDRIVE = 10b		2000		
		TDRIVE = 11b		4000		
t_{DRIVE}	Peak gate drive time (HW Device)			4000		ns

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEP}	Peak source gate current (high-side and low-side) (SPI Device)	IDRIVEP_HS or IDRIVEP__LS = 000b		15		mA
		IDRIVEP_HS or IDRIVEP__LS = 001b		15		
		IDRIVEP_HS or IDRIVEP__LS = 010b		45		
		IDRIVEP_HS or IDRIVEP__LS = 011b		60		
		IDRIVEP_HS or IDRIVEP__LS = 100b		90		
		IDRIVEP_HS or IDRIVEP__LS = 101b		105		
		IDRIVEP_HS or IDRIVEP__LS = 110b		135		
		IDRIVEP_HS or IDRIVEP__LS = 111b		150		
I_{DRIVEP}	Peak source gate current (high-side and low-side) (HW Device)	IDRIVE tied to AGND		15		mA
		IDRIVE 18 kΩ (±5%) to AGND		45		
		IDRIVE 75 kΩ (±5%) to AGND		60		
		IDRIVE Hi-Z (> 500 kΩ to AGND)		90		
		IDRIVE 75 kΩ (±5%) to DVDD		105		
		IDRIVE 18 kΩ (±5%) to DVDD		135		
		IDRIVE tied to DVDD		150		
I_{DRIVEN}	Peak sink gate current (high-side and low-side) (SPI Device)	IDRIVEN_HS or IDRIVEN_LS = 000b		30		mA
		IDRIVEN_HS or IDRIVEN_LS = 001b		30		
		IDRIVEN_HS or IDRIVEN_LS = 010b		90		
		IDRIVEN_HS or IDRIVEN_LS = 011b		120		
		IDRIVEN_HS or IDRIVEN_LS = 100b		180		
		IDRIVEN_HS or IDRIVEN_LS = 101b		210		
		IDRIVEN_HS or IDRIVEN_LS = 110b		270		
		IDRIVEN_HS or IDRIVEN_LS = 111b		300		
I_{DRIVEN}	Peak sink gate current (high-side and low-side) (HW Device)	IDRIVE tied to AGND		30		mA
		IDRIVE 18 kΩ (±5%) to AGND		90		
		IDRIVE 75 kΩ (±5%) to AGND		120		
		IDRIVE Hi-Z (> 500 kΩ to AGND)		180		
		IDRIVE 75 kΩ (±5%) to DVDD		210		
		IDRIVE 18 kΩ (±5%) to DVDD		270		
		IDRIVE tied to DVDD		300		
I_{HOLD}	FET holding current	Source current after t_{DRIVE}		15		mA
		Sink current after t_{DRIVE}		30		
I_{STRONG}	FET hold-off strong pulldown	GLX pull-down current during GHX t_{DRIVE} period or vice-versa		300		mA
R_{OFF}	FET gate hold-off resistor	GHX to SHX and GLX to PGND		150		kΩ
t_{PD}	Propagation delay	INHX/INLX tansition to GHX/GLX transition		180	250	ns
CURRENT SHUNT AMPLIFIERS (SNx, SOx, SPx, VREF)						
G_{CSA}	Amplifier gain (SPI Device)	CSA_GAIN = 00b, VREF = 3.3 to 5 V	4.85	5	5.15	V/V
		CSA_GAIN = 01b, VREF = 3.3 to 5 V	9.7	10	10.3	
		CSA_GAIN = 10b, VREF = 3.3 to 5 V	19.4	20	20.6	
		CSA_GAIN = 11b, VREF = 3.3 to 5 V	38.8	40	41.2	
G_{CSA}	Amplifier gain (HW Device)	Tied to AGND, VREF = 3.3 to 5 V	4.85	5	5.15	V/V
		45 kΩ ± 5% to AGND, VREF = 3.3 to 5 V	9.7	10	10.3	
		Hi-Z, VREF = 3.3 to 5 V	19.4	20	20.6	
		Tied to DVDD, VREF = 3.3 to 5 V	38.8	40	41.2	

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET} (1)	Settling time to ±1%, 30 pF	STEP on SOX = 0.5 V; G_{CSA} = 5 V/V, VREF = 3.3 to 5 V		260		ns
		STEP on SOX = 0.5 V; G_{CSA} = 10 V/V, VREF = 3.3 to 5 V		400		
		STEP on SOX = 0.5 V; G_{CSA} = 20 V/V, VREF = 3.3 to 5 V		700		
		STEP on SOX = 0.5 V; G_{CSA} = 40 V/V, VREF = 3.3 to 5 V		1550		
$V_{SP, COM}$ (1)	Common-mode input range		–0.5		0.5	V
V_{OFF}	Input offset error	V_{SP} = V_{SN} = 0 V, G_{CSA} = 5, VREF = 3.3 V ± 10%	–5		5	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 10, VREF = 3.3 V ± 10%	–2.5		2.5	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 20, VREF = 3.3 V ± 10%	–1.5		1.5	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 40, VREF = 3.3 V ± 10%	–1.25		1.25	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 5, VREF = 5 V ± 10%	–7		7	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 10, VREF = 5 V ± 10%	–3.5		3.5	mV
		V_{SP} = V_{SN} = 0 V, G_{CSA} = 20, VREF = 5 V ± 10%	–2.25		2.25	mV
		V_{SP} = V_{SN} = 0 V, GCSA = 40, VREF = 5 V ± 10%	–1.5		1.5	mV
V_{DRIFT} (1)	Drift offset	V_{SP} = V_{SN} = 0 V		10		µV/°C
V_{LINEAR} (1)	SOX output voltage linear range		0.25		V_{VREF} – 0.25	V
V_{BIAS}	SOX output voltage bias (SPI Device)	V_{SP} = V_{SN} = 0 V, VREF_DIV = 0b		V_{VREF} – 0.3		V
		V_{SP} = V_{SN} = 0 V, VREF_DIV = 1b		V_{VREF}/2		
V_{BIAS}	SOX output voltage bias (HW Device)	V_{SP} = V_{SN} = 0 V		V_{VREF}/2		V
I_{BIAS}	SPX/SNX negative input bias current	V_{SP} = V_{SN} = 0 V			200	µA
V_{REFUV}	VREF undervoltage			2.6		V
I_{VREF}	VREF input current	VREF = 5.0 V		1	2	mA
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	VM falling, UVLO report	5.4		5.8	V
		VM rising, UVLO recovery	5.6		6	
V_{UVLO_HYS}	VM undervoltage hysteresis	Rising to falling threshold		200		mV
t_{UVLO_DEG} (1)	VM undervoltage deglitch time	VM falling, UVLO report		10		µs
V_{CPUV}	Charge pump undervoltage	With respect to VM		2.4		V
V_{GS_CLAMP}	Gate drive clamping voltage	Positive clamping voltage	10.5		15	V
		Negative clamping voltage		–0.6		
V_{DS_OCP}	V_{DS} overcurrent trip voltage (SPI Device)	VDS_LVL = 000b		0.15		V
		VDS_LVL = 001b		0.24		
		VDS_LVL = 010b		0.4		
		VDS_LVL = 011b		0.51		
		VDS_LVL = 100b		0.6		
		VDS_LVL = 101b		0.9		
		VDS_LVL = 110b		1.8		
		VDS_LVL = 111b		Disabled		

Electrical Characteristics (continued)

at V_{VM} = 6 to 38 V over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DS_OCP}	V_{DS} overcurrent trip voltage (HW Device)	VDS tied to AGND		0.15		V
		VDS 18 kΩ (±5%) to AGND		0.24		
		VDS 75 kΩ (±5%) to AGND		0.4		
		VDS Hi-Z (> 500 kΩ to AGND)		0.6		
		VDS 75 kΩ (±5%) to DVDD		0.9		
		VDS 18 kΩ (±5%) to DVDD		1.8		
		VDS tied to DVDD		Disabled		
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage (SPI Device)	SEN_LVL = 00b		0.25		V
		SEN_LVL = 01b		0.5		
		SEN_LVL = 10b		0.75		
		SEN_LVL = 11b		1		
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage (HW Device)			1		V
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time			4.5		µs
t_{RETRY}	Overcurrent retry time (SPI Device)	TRETRY = 0b		4		ms
		TRETRY = 1b		500		µs
t_{RETRY}	Overcurrent retry time (HW Device)			4		ms
T_{OTW} (1)	Thermal warning temperature	Die temperature (T_j)	120	140		°C
T_{OTSD} (1)	Thermal shutdown temperature	Die temperature (T_j)	150	170		°C
T_{HYS} (1)	Thermal hysteresis	Die temperature (T_j)		20		°C

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SPI (nSCS, SCLK, SDI, SDO)						
t_{READY}	SPI ready after after enable	VM > UVLO, ENABLE = 3.3 V			1	ms
t_{CLK}	SCLK minimum period		200			ns
t_{CLKH}	SCLK minimum high time		100			ns
t_{CLKL}	SCLK minimum low time		100			ns
t_{SU_SDI}	SDI input data setup time		40			ns
t_{HD_SDI}	SDI input data hold time		60			ns
t_{DLY_SDO}	SDO output data delay time	SCLK high to SDO valid			60	ns
t_{SU_nSCS}	nSCS input setup time		100			ns
t_{HD_nSCS}	nSCS input hold time		100			ns
t_{HI_nSCS}	nSCS minimum high time before active low		600			ns
t_{EN_nSCS}	nSCS enable time	nSCS low to SDO out of high impedance		20		ns
t_{DIS_nSCS}	nSCS disable delay time	nSCS high to SDO high impedance		20		ns

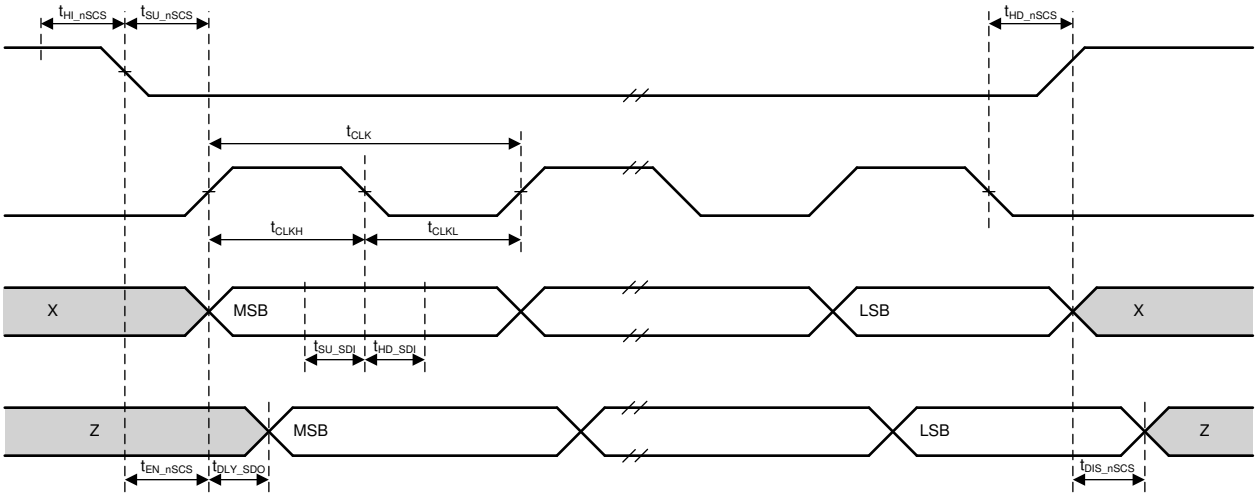


Figure 1. SPI Slave-Mode Timing Diagram

6.7 Typical Characteristics

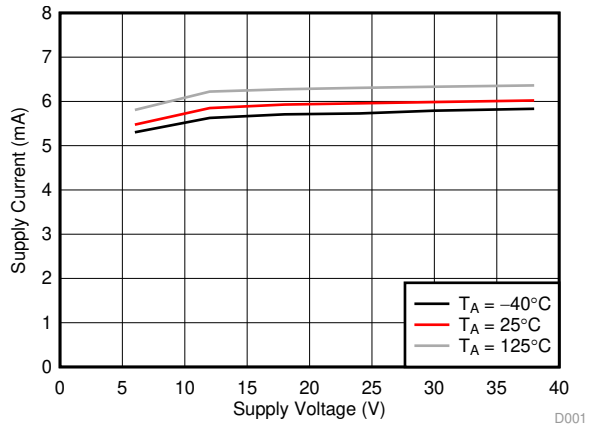


Figure 2. Supply Current Over Supply Voltage

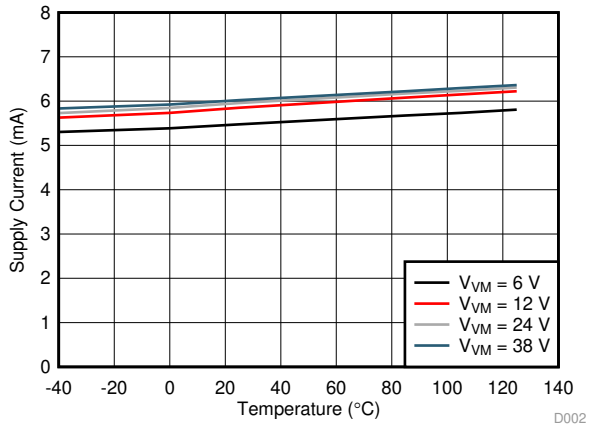


Figure 3. Supply Current Over Temperature

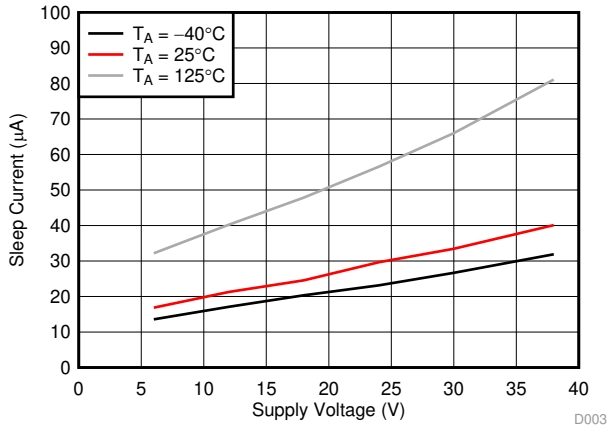


Figure 4. Sleep Current Over Supply Voltage

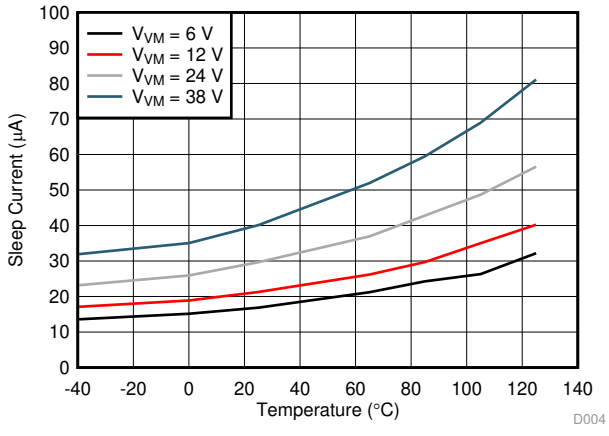
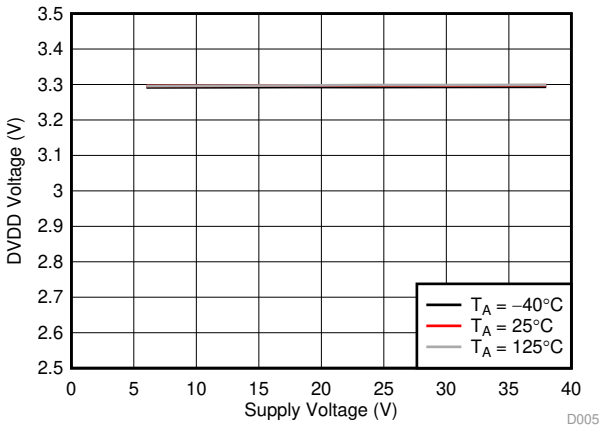


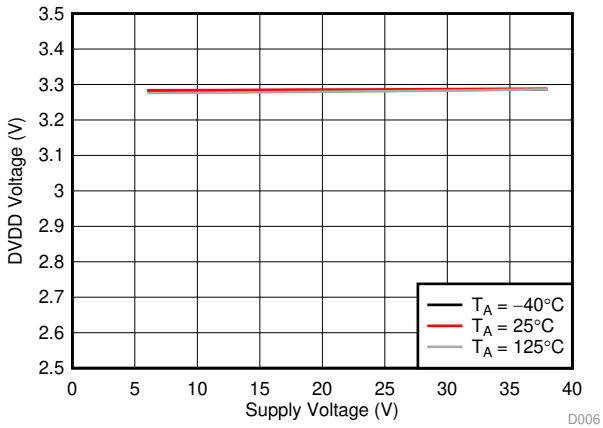
Figure 5. Sleep Current Over Temperature

Typical Characteristics (continued)



I_{DVDD} = 0 mA

Figure 6. DVDD Voltage Over Supply Voltage



I_{DVDD} = 30 mA

Figure 7. DVDD Voltage Over Supply Voltage

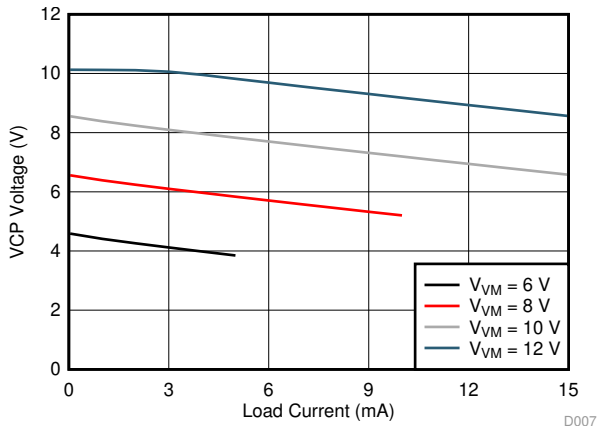


Figure 8. VCP Voltage Over Load

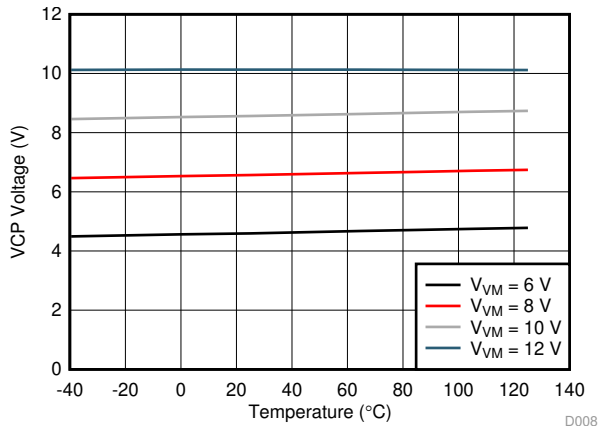


Figure 9. VCP Voltage Over Temperature

7 Detailed Description

7.1 Overview

The DRV8304 device is an integrated 6-V to 38-V gate driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three independent half-bridge gate drivers, charge pump, and linear regulator for the high-side and low-side gate-driver supply voltages. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 150-mA source, 300-mA sink peak currents with a 15-mA average output current. The high-side gate-drive supply voltage is generated using a doubler charge-pump architecture that regulates the VCP output to V_{VM} + 10 V. The low-side gate-drive supply voltage is generated using a linear regulator from the VM power supply that regulates to 10 V. A smart gate-drive (SGD) architecture provides the ability to dynamically adjust the output gate-drive current strength allowing for the gate driver to control the power MOSFET V_{DS} switching speed. This feature allows for the removal of external gate-drive resistors and diodes reducing bill of materials (BOM) component count, cost, and printed circuit board (PCB) area. The architecture also uses an internal state machine to protect against gate-drive short-circuit events, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

The DRV8304 device integrates three, bidirectional current-shunt amplifiers for monitoring the current level through each of the external half-bridges using a low-side shunt resistor. The gain setting of the shunt amplifier can be adjusted through the SPI (DRV8304S) or hardware (DRV8304H) interface with the SPI providing additional flexibility to adjust the output bias point.

In addition to the high level of device integration, the DRV8304 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), V_{DS} overcurrent monitoring (OCP), gate-driver short-circuit detection (GDF), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV8304 device is available in 0.5-mm pin pitch, VQFN surface-mount packages. The VQFN package size is 6 mm × 6 mm.

7.2 Functional Block Diagram

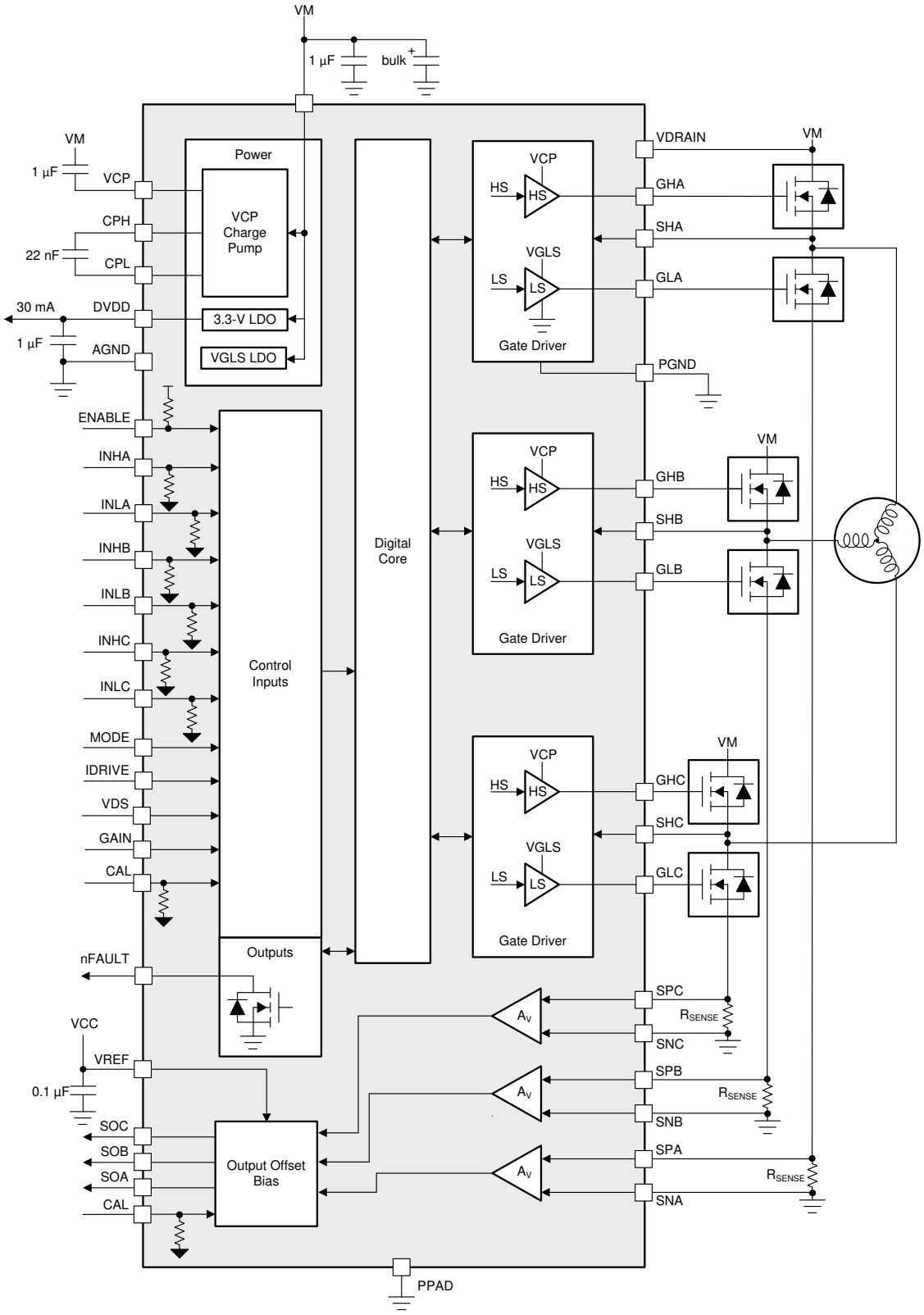


Figure 10. Block Diagram for DRV8304H

Functional Block Diagram (continued)

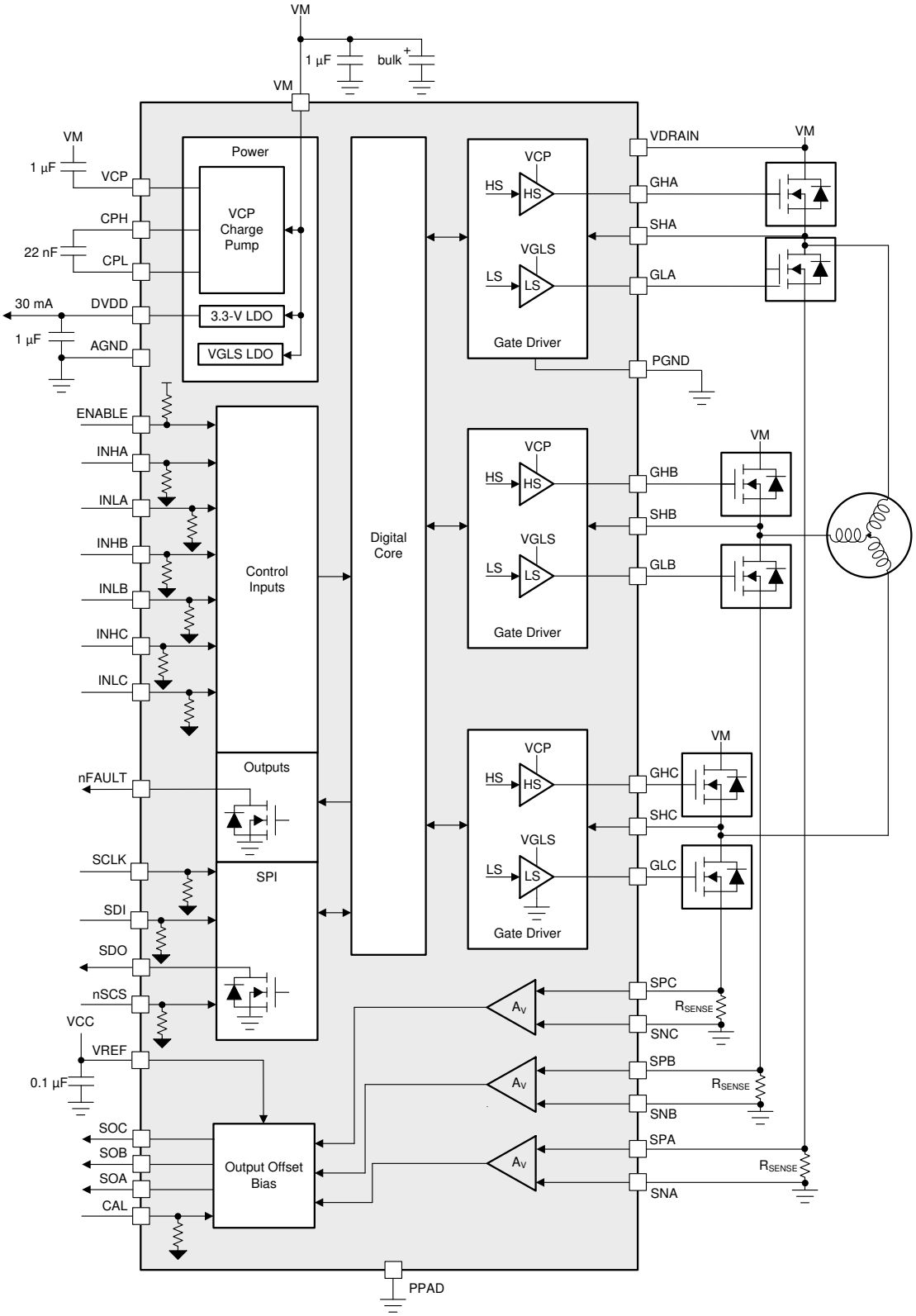


Figure 11. Block Diagram for DRV8304S

7.3 Feature Description

Table 1 lists the recommended values of the external components for the gate driver.

Table 1. DRV8304 Gate-Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	PGND	≥ 10 µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{SW}	CPH	CPL	X5R or X7R, 22-nF, VM-rated capacitor
C_{DVDD}	DVDD	AGND	X5R or X7R, 1-µF, 6.3-V capacitor
R_{nFAULT}	VCC (1)	nFAULT	5.1-kΩ, Pullup resistor
R_{SDO}	VCC (1)	SDO	5.1-kΩ, Pullup resistor, DRV8304 SPI device
R_{IDRIVE}	IDRIVE	AGND or DVDD	DRV8304 hardware interface
R_{VDS}	VDS	AGND or DVDD	DRV8304 hardware interface
R_{MODE}	MODE	AGND or DVDD	DRV8304 hardware interface
R_{GAIN}	GAIN	AGND or DVDD	DRV8304 hardware interface
C_{VREF}	VREF	AGND or DGND	X5R or X7R, 0.1-µF, VREF-rated capacitor (Optional)
R_{ASENSE}	SPA	SNA and PGND	Sense shunt resistor based on current regulation limit
R_{BSENSE}	SPB	SNB and PGND	Sense shunt resistor based on current regulation limit
R_{CSENSE}	SPC	SNC and PGND	Sense shunt resistor based on current regulation limit

(1) The VCC pin is not a pin on the DRV8304 device, but a VCC supply voltage pullup is required for the open-drain output nFAULT and SDO. These pins can also be pulled up to DVDD.

7.3.1 3-Phase Smart Gate Drivers

The DRV8304 device integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A doubler charge pump provides the proper gate-bias voltage to the high-side MOSFET across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The half-bridge gate drivers can be used in combination to drive a 3-phase motor or separately to drive other types of loads.

The DRV8304 device implements a smart gate-drive architecture which allows the user to dynamically adjust the gate drive current without requiring external gate current limiting resistors. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead-time insertion, parasitic dV/dt gate turnon prevention, and gate-fault detection.

7.3.1.1 PWM Control Modes

The DRV8304 device provides four different PWM-control modes to support various commutation and control methods. Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs.

7.3.1.1.1 6x PWM Mode (PWM_MODE = 00b or MODE Pin Tied to AGND)

In this mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 2.

Table 2. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

7.3.1.1.2 3x PWM Mode (PWM_MODE = 01b or MODE Pin = 47 kΩ to AGND)

In this mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to change the half-bridge to high impedance. If the high-impedance (Hi-Z) sate is not required, tie all INLx pins logic high. The corresponding INHx and INLx signals control the output state as listed in Table 3.

Table 3. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

7.3.1.1.3 1x PWM Mode (PWM_MODE = 10b or MODE Pin = Hi-Z)

In this mode, the DRV8304 device uses 6-step block commutation tables that are stored internally. This feature allows for a 3-phase BLDC motor to be controlled using a single PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to hall sensor digital outputs from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode normally operates with synchronous rectification, however it can be configured to use asynchronous diode freewheeling rectification on the SPI device. This configuration is set using the 1PWM_COM bit through the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when hall sensors are directly controlling the INLA, INHB, and INLB state inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled low. This brake is independent of the states of the other input pins. Tie the INLC pin high if this feature is not required.

Table 4. Synchronous 1x PWM Mode

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

Table 5. Asynchronous 1x PWM Mode 1PWM_COM = 1 (SPI Only)

LOGIC AND HALL INPUTS							GATE-DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 12 and Figure 13 show the different possible configurations in 1x PWM mode.

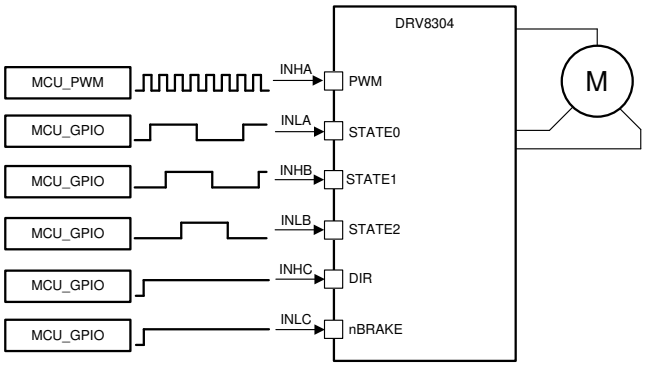


Figure 12. 1x PWM—Simple Controller

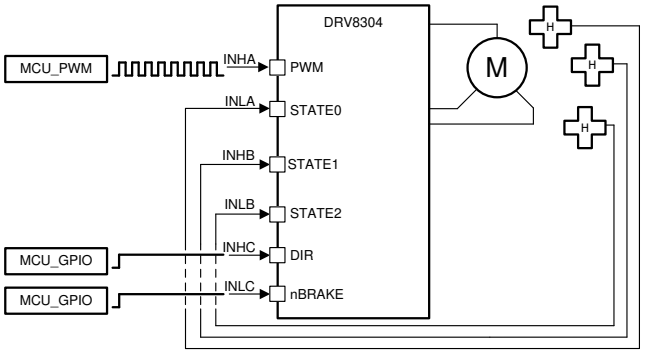


Figure 13. 1x PWM—Hall Sensor

7.3.1.1.4 Independent PWM Mode (PWM_MODE = 11b or MODE Pin Tied to DVDD)

In this mode, the corresponding input pin independently controls each high-side and low-side gate driver. This control mode allows for the DRV8304 device to drive separate high-side and low-side loads with each half-bridge. These types of loads include unidirectional brushed DC motors, solenoids, and low-side and high-side switches. In this mode, if the system is configured in a half-bridge configuration, simultaneously turning on both the high-side and low-side MOSFETs causes shoot-through current in external MOSFETs and can cause them to damage.

Table 6. Independent PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Because the high-side and low-side V_{DS} overcurrent monitors share the SHx sense line, using the monitors if both the high-side and low-side gate drivers of one half-bridge are split and being used is not possible. In this case, connect the SHx pin to the high-side driver and disable the V_{DS} overcurrent monitors as shown in Figure 14.

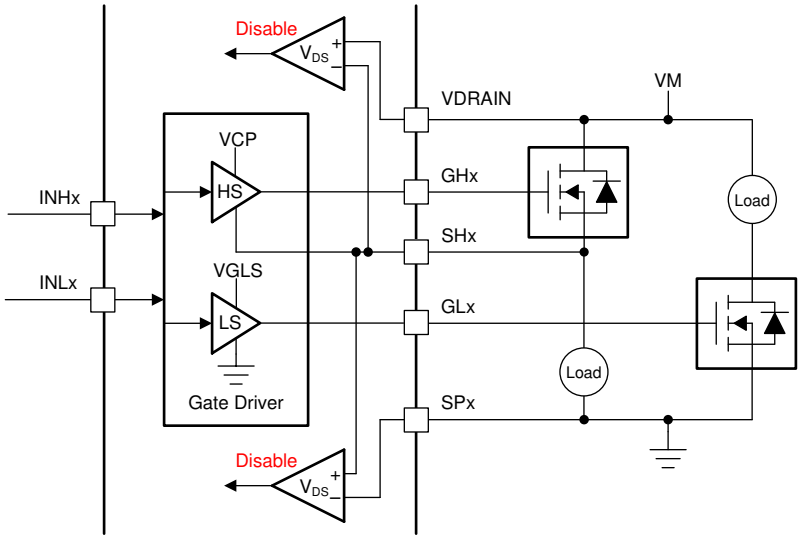


Figure 14. Independent PWM High-Side and Low-Side Drivers

If the half-bridge is used to implement only a high-side or low-side driver, using the V_{DS} overcurrent monitors is still possible. Connect the SHx pin as shown in Figure 15 or Figure 16. The unused gate driver and the corresponding input can be left disconnected.

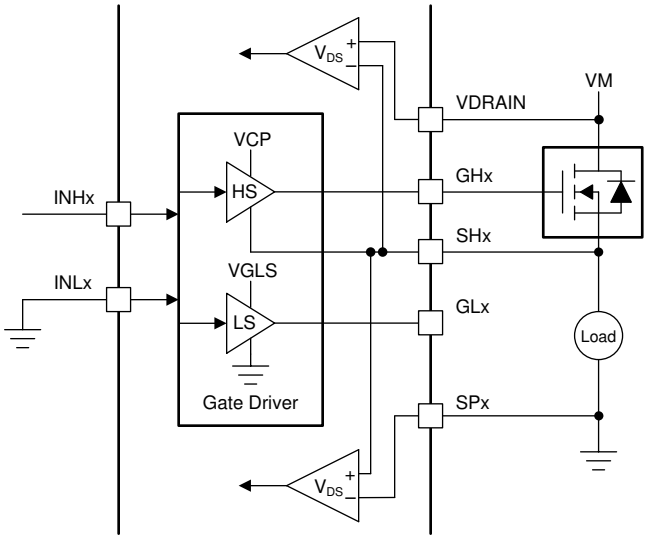


Figure 15. Single High-Side Driver

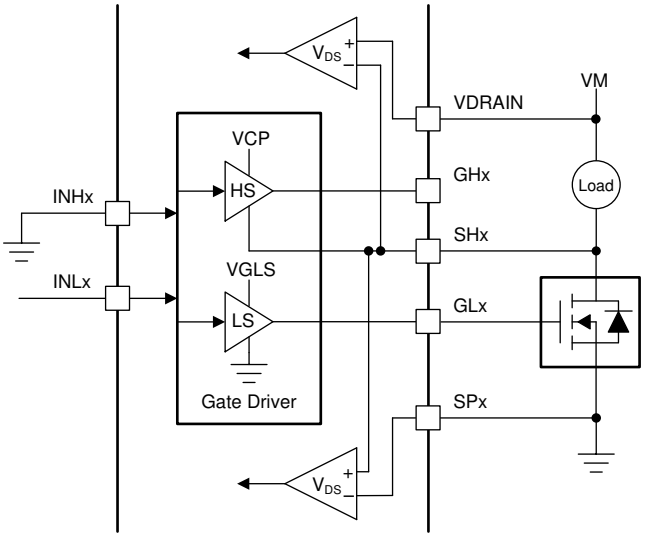


Figure 16. Single Low-Side Driver

7.3.1.2 Device Interface Modes

The DRV8304 device supports two different interface modes (SPI and hardware) to allow the end application to design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This allows for application designers to evaluate with one interface version and potentially switch to another with minimal modifications to their design.

7.3.1.2.1 Serial Peripheral Interface (SPI)

The SPI device supports a serial communication bus that allows for an external controller to send and receive data with the DRV8304 device. This bus allows for the external controller to configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins.

- The SCLK pin is an input which accepts a clock signal to determine when data is captured and propagated on SDI and SDO.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8304 device.

For more information on the SPI, see the *SPI Communication* section.

7.3.1.2.2 Hardware Interface

The hardware interface device converts the four SPI pins into four resistor configurable inputs, GAIN, IDRIVE, MODE, and VDS. This option allows for the application designer to configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This configuration removes the requirement for a SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the current shunt-amplifier gain.
- The IDRIVE pin configures the gate-drive current strength.
- The MODE pin configures the PWM control mode.
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see the *Pin Diagrams* section.

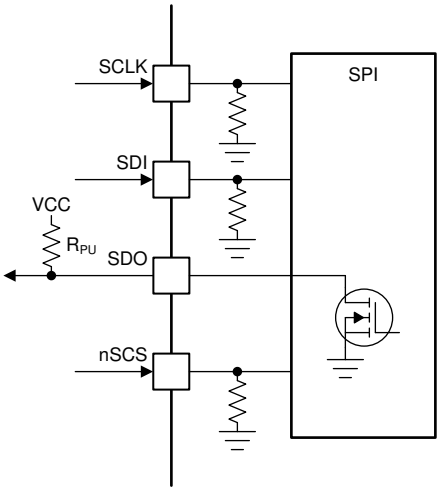


Figure 17. SPI

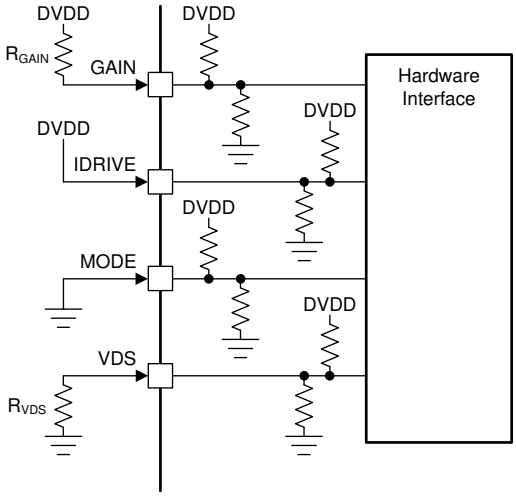


Figure 18. Hardware Interface

7.3.1.3 Gate Driver Voltage Supplies

The high-side gate-drive voltage supply is created using a doubler charge pump that operates from the VM voltage supply input. The charge pump allows the gate driver to properly bias the high-side MOSFET gate with respect to the source across a wide input supply-voltage range. The charge pump is regulated to maintain a fixed output voltage of V_{VM} + 10 V and supports an average output current of 15 mA. When V_{VM} is less than 12 V, the charge pump operates in full doubler mode and generates $V_{VCP} = 2 \times V_{VM} - 1.5$ V when unloaded. The charge pump is continuously monitored for undervoltage to prevent under-driven MOSFET conditions. The charge pump requires a X5R or X7R, 1-µF, 16-V ceramic capacitor between the VM and VCP pins to act as the storage capacitor. Additionally, a X5R or X7R, 22-nF, VM-rated ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

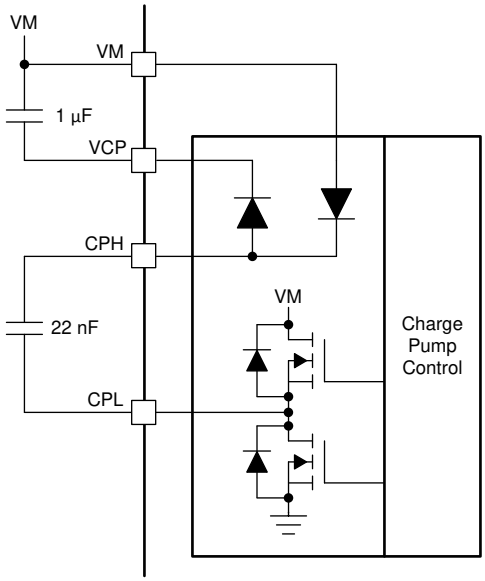


Figure 19. Charge Pump Architecture

The low-side gate-drive voltage is created using a linear regulator that operates from the VM voltage supply input. The linear regulator allows the gate driver to properly bias the low-side MOSFET gate with respect to ground. The linear regulator output is fixed at 10 V and supports an output current of 15 mA.

7.3.1.4 Smart Gate-Drive Architecture

The DRV8304 gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

Additionally, the gate drivers use a smart gate-drive architecture to provide additional control of the external power MOSFETs, take additional steps to protect the MOSFETs, and allow for optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called I_{DRIVE} and T_{DRIVE} which are detailed in the *IDRIVE: MOSFET Slew-Rate Control* section and *TDRIVE: MOSFET Gate Drive Control* section. Figure 20 shows the high-level functional block diagram of the gate driver.

The I_{DRIVE} gate-drive current and T_{DRIVE} gate-drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see the *Application and Implementation* section).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

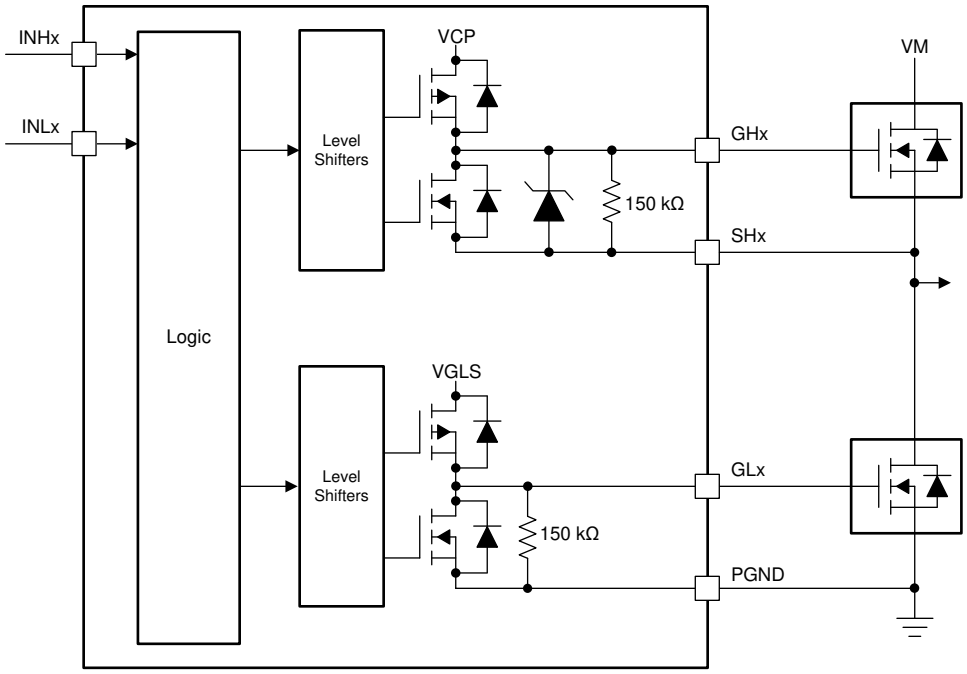


Figure 20. Gate Driver Block Diagram

7.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate-drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, dV/dt gate turnon leading to shoot-through, and switching voltage transients related to parasitics in the external half-bridge. IDRIVE operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{gd} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV8304 device to dynamically switch between gate drive currents either through a register setting on the SPI device or the IDRIVE pin on hardware interface device. The SPI and hardware devices provide 7 I_{DRIVE} settings ranging from 15-mA to 150-mA source and 30-mA to 300-mA sink. The gate-drive current setting is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold current (I_{HOLD}) to improve the gate driver efficiency. Additional details on the IDRIVE settings are described in the *Register Maps* section for the SPI device and in the *Pin Diagrams* section for the hardware interface device.

7.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate-drive state machine that provides automatic dead-time insertion through switching handshaking, parasitic dV/dt gate turnon prevention, and MOSFET gate-fault detection.

The first component of the TDRIVE state machine is automatic dead-time insertion. Dead time is the period of time between the switching of the external high-side and low-side MOSFETs to ensure that they do not cross conduct and cause shoot-through. The DRV8304 device uses the V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the proper time to switch instead of relying on a fixed time value. This feature allows the gate-driver dead time to adjust for variation in the system such a temperature drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) can be inserted and is adjustable through the registers on the SPI device.

The second component focuses on parasitic dV/dt gate turnon prevention. To implement this, the TDRIVE state machine enables a strong pulldown current (I_{STRONG}) on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown happens for the t_{DRIVE} duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the half-bridge switch-node voltage slews rapidly.

The third component implements a gate-fault detection scheme to detect pin-to-pin solder defects, a MOSFET gate failure, or a MOSFET gate stuck-high or stuck-low voltage condition. This implementation is done with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge it begins to monitor the gate voltage of the external MOSFET. If, at the end of the t_{DRIVE} period, the V_{GS} voltage has not reached the proper threshold, the gate driver reports a fault. To ensure that a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. Additional details on the TDRIVE settings are described in the *Register Maps* section for SPI device and in the *Pin Diagrams* section for hardware interface device.

NOTE

If the mode is set to independent PWM mode, then the IDRIVE current is automatically set for the IHOLD period.

Figure 21 shows an example of the TDRIVE state machine in operation.

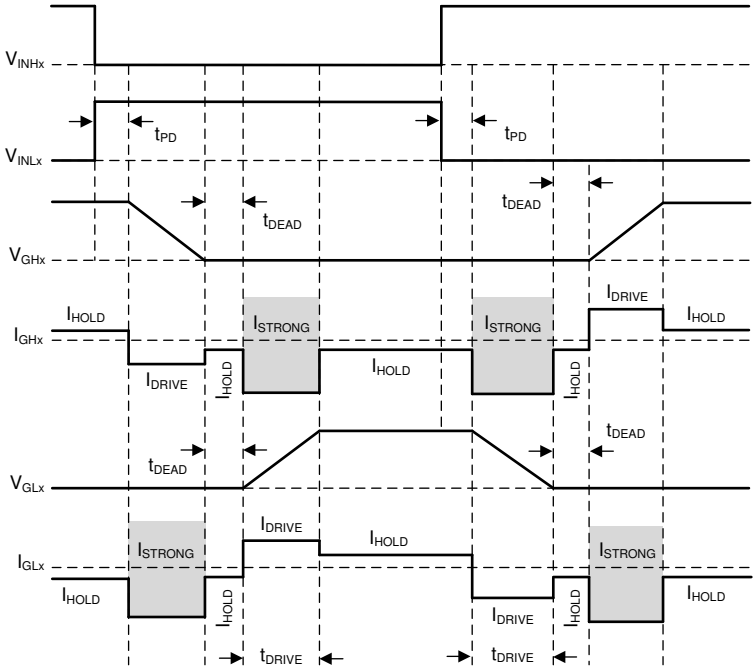


Figure 21. TDRIVE State Machine

7.3.1.4.3 Gate Drive Clamp

A clamping structure limits the gate-drive output voltage to the $V_{GS,CLAMP}$ voltage to help protect the external high-side MOSFETs from gate overvoltage damage. The positive voltage clamp is realized using a series of diodes. The negative voltage clamp uses the body diodes of the internal pulldown gate driver as shown in Figure 22.

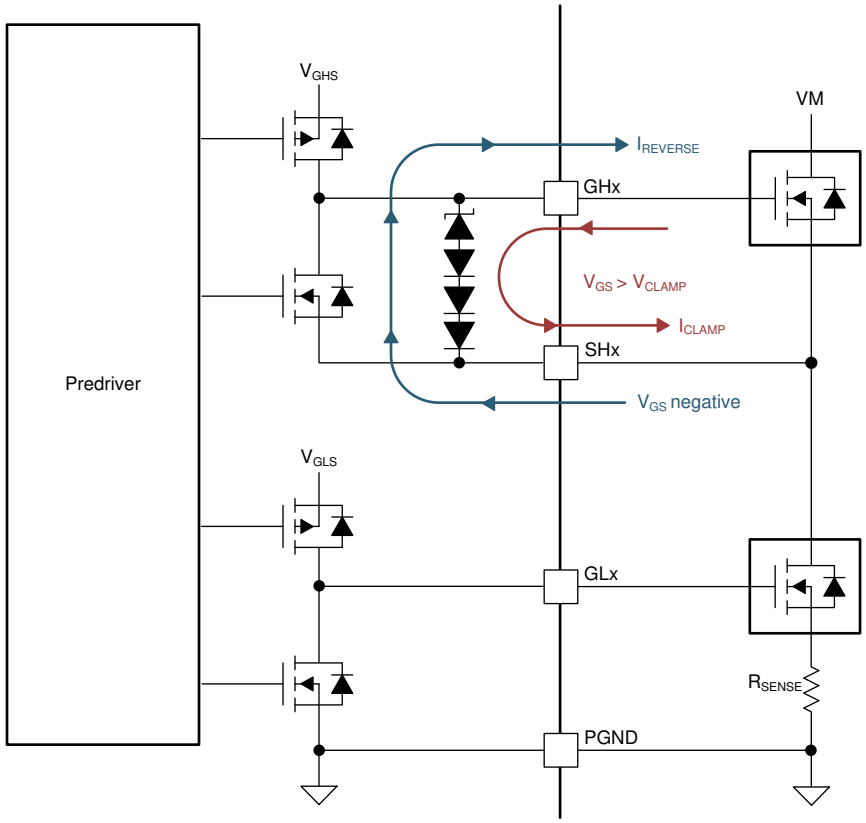


Figure 22. Gate Drive Clamp

7.3.1.4.4 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time comprises three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead-time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

In order for the output to change state during normal operation, one MOSFET must first be turned off. The MOSFET gate is ramped down according to the IDRIVE setting, and the observed propagation delay ends when the MOSFET gate falls below the threshold voltage.

7.3.1.4.5 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device V_{DS} fault mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins and the low-side V_{DS} monitors measure the voltage between the SHx and SPx pins. If the current shunt amplifier is unused, tie the SP pins to the common ground point of the external half-bridges.

For the SPI device, the reference point of the low-side V_{DS} monitor can be changed between the SPx and SNx pins if desired with the LS_REF register setting.

The V_{VDS_OCP} threshold is programmable from 0.15 V to 1.8 V. Additional information on the V_{DS} monitor levels are described in the *Register Maps* section for the SPI device and in the *Pin Diagrams* section hardware interface device.

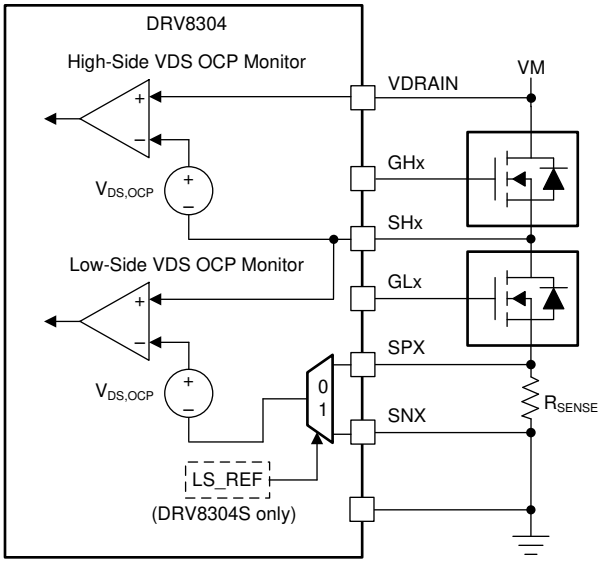


Figure 23. DRV8304 V_{DS} Monitors

7.3.1.4.6 VDRAIN Sense Pin

The DRV8304 device provides a separate sense pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin allows the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) to remain separate and prevent noise on the VDRAIN sense line. This separation also allows for a small filter to be implemented on the gate driver supply (VM) or to insert a boost converter to support lower voltage operation if desired. Care must still be taken when the filter or separate supply is designed because the VM supply is still the reference point for the VCP charge pump that supplies the high-side gate drive voltage (V_{GSH}). The VM supply must not drift to far from the VDRAIN supply to avoid violating the V_{GS} voltage specification of the external power MOSFETs.

7.3.2 DVDD Linear Voltage Regulator

A 3.3-V, 30-mA linear regulator is integrated into the DRV8304 device and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power microcontroller or other low-current supporting circuitry. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The DVDD nominal, no-load output voltage is 3.3 V. When the DVDD load current exceeds 30 mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 30 mA.

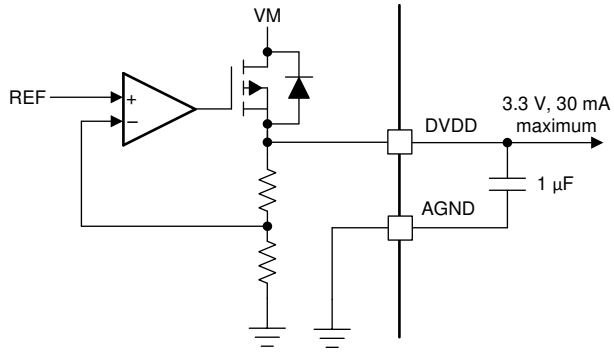


Figure 24. DVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device because of the DVDD linear regulator.

$$P = (V_{VM} - V_{DVDD}) \times I_{DVDD} \quad (1)$$

For example, at V_{VM} = 24 V, drawing 20 mA out of DVDD results in a power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

7.3.3 Pin Diagrams

Figure 25 shows the input structure for the logic-level pins, INHx, INLx, CAL, nSCS, SCLK, and SDI. The input can be driven with a voltage or external resistor.

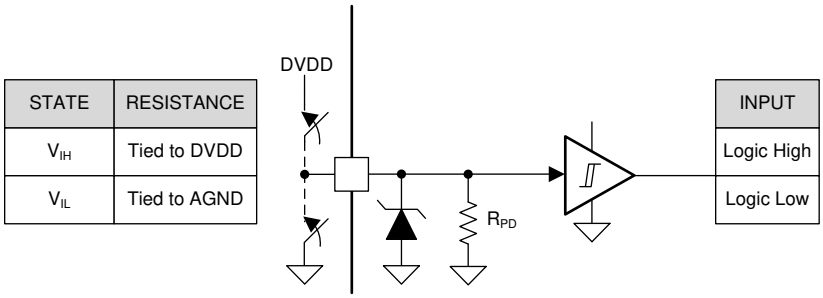


Figure 25. Logic-Level Input Pin Structure (INHx, INLx, CAL, nSCS, SCLK, and SDI)

Figure 26 shows the input structure for the logic-level ENABLE pin. The input can be driven with a voltage or external resistor. The ENABLE pin is latched when the device is powered-up.

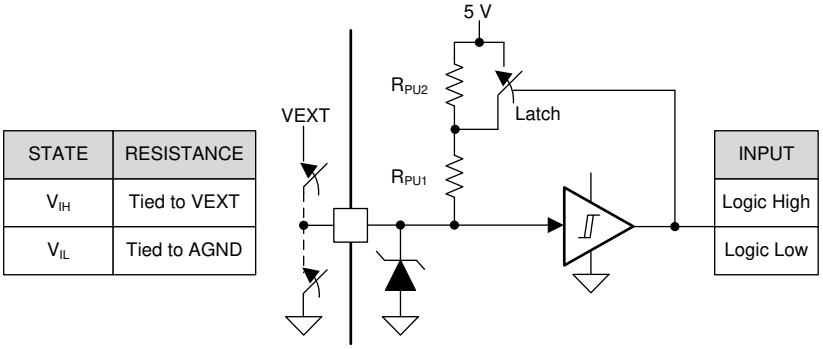


Figure 26. Logic-Level Input Pin Structure (ENABLE)

Figure 27 shows the structure of the four-level input pins, MODE and GAIN, on the hardware interface device. The input can be set with an external resistor. The MODE and GAIN pins are latched when the device is powered-up.

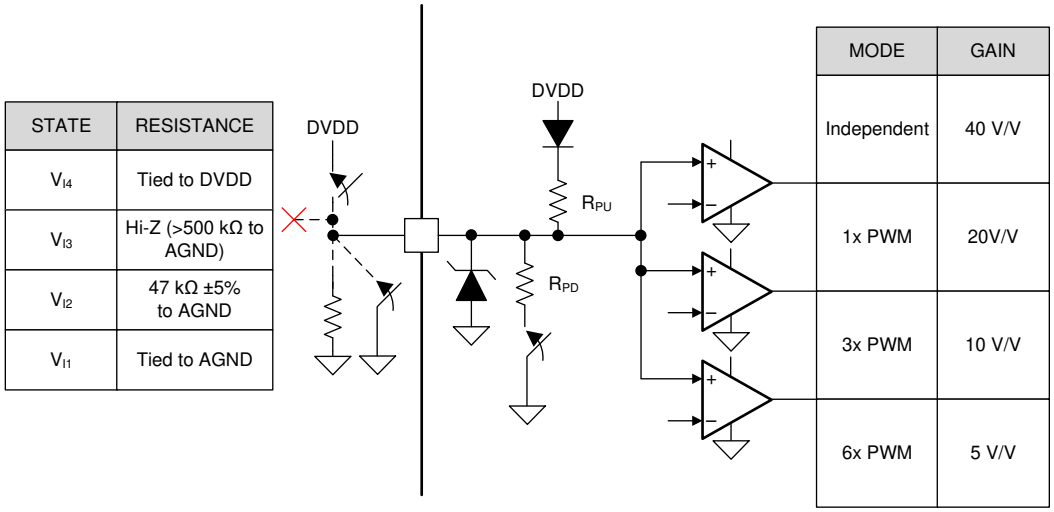


Figure 27. Four-Level Input Pin Structure (MODE and GAIN)

Figure 28 shows the structure of the seven-level input pins, IDRIVE and VDS, on the hardware interface device. The input can be set with an external resistor. The IDRIVE and VDS pins are latched when the device is powered-up.

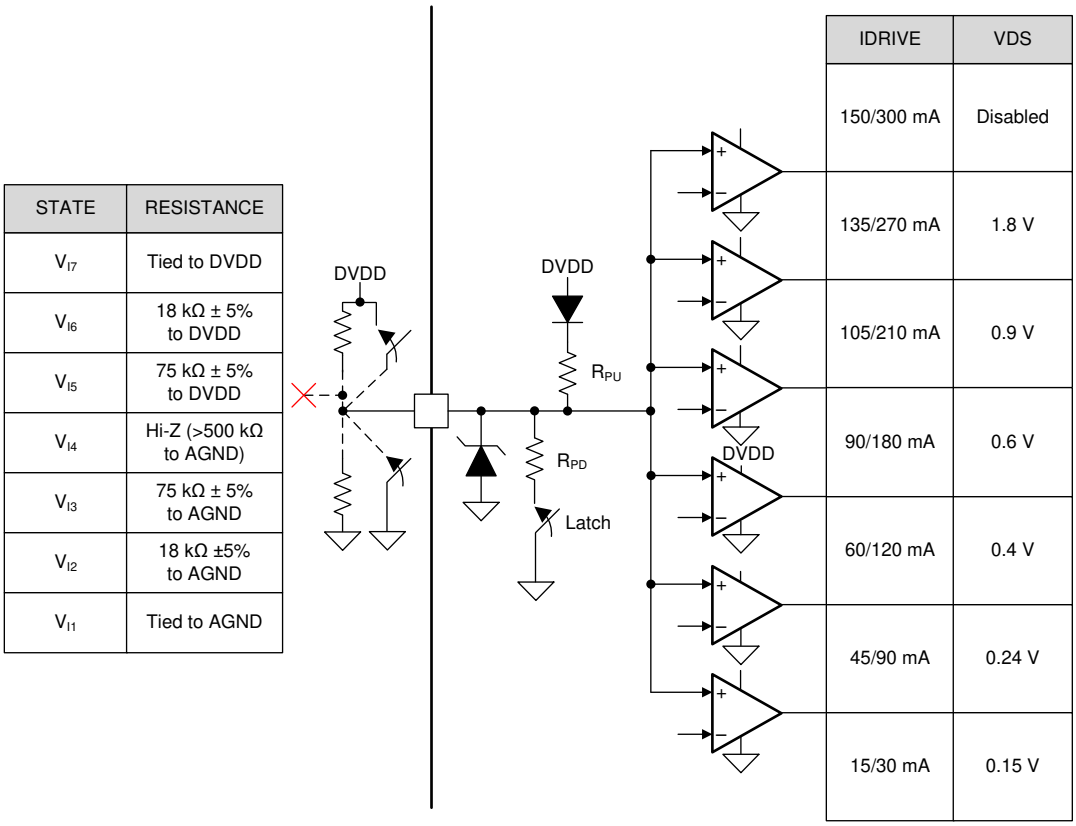


Figure 28. Seven-Level Input Pin Structure (IDRIVE and VDS)

Figure 29 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function properly.

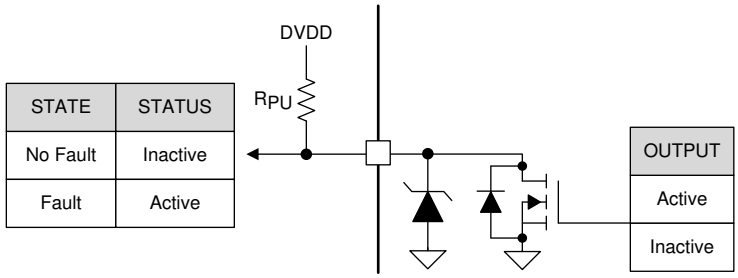


Figure 29. Open-Drain Output Pin Structure

7.3.4 Low-Side Current-Shunt Amplifiers

The DRV8304 device integrates three, high-performance low-side current-shunt amplifiers for current measurements using low-side shunt resistors in the external half-bridges. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs or one amplifier can be used to sense the sum of the half-bridge legs. The current shunt amplifiers include features such as programmable gain, offset calibration, unidirectional and bidirectional support, and a voltage reference pin (VREF).

7.3.4.1 Bidirectional Current Sense Operation

The SOx pin on the DRV8304 outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}) as shown in Figure 30. The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). Use Equation 3 to calculate the current through the shunt resistor.

$$I = \frac{\frac{V_{VREF}}{2} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \quad (3)$$

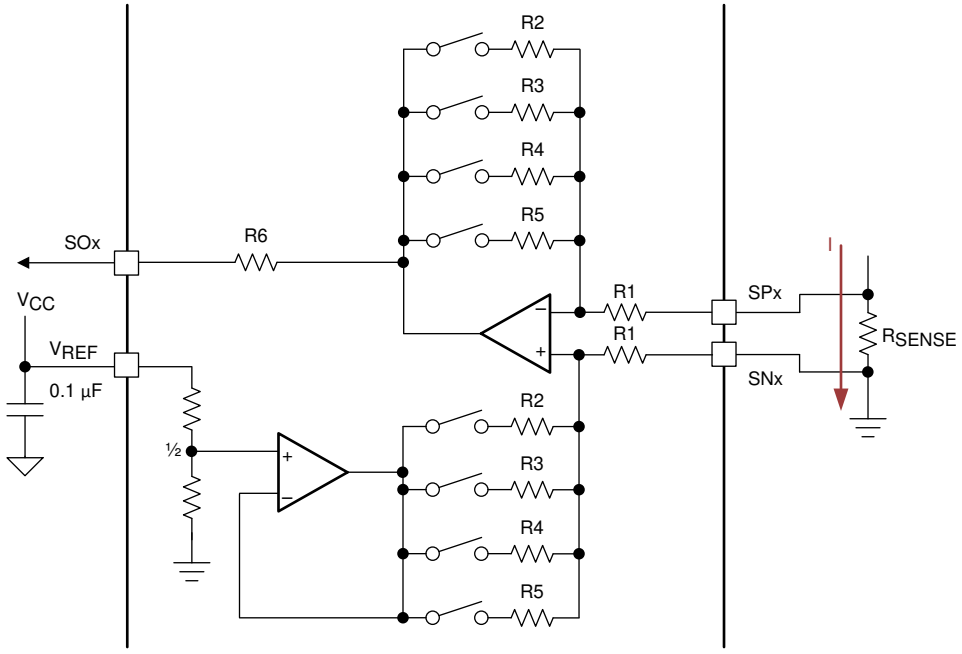


Figure 30. Bidirectional Current-Sense Configuration

Figure 31 and Figure 32 show the detail of the amplifier operational range. In bi-directional operation, the amplifier output for 0-V input is set at VREF / 2. Any change in the differential input results in a corresponding change in the output times the CSA_GAIN factor. The amplifier has a defined linear region in which it can maintain operation.

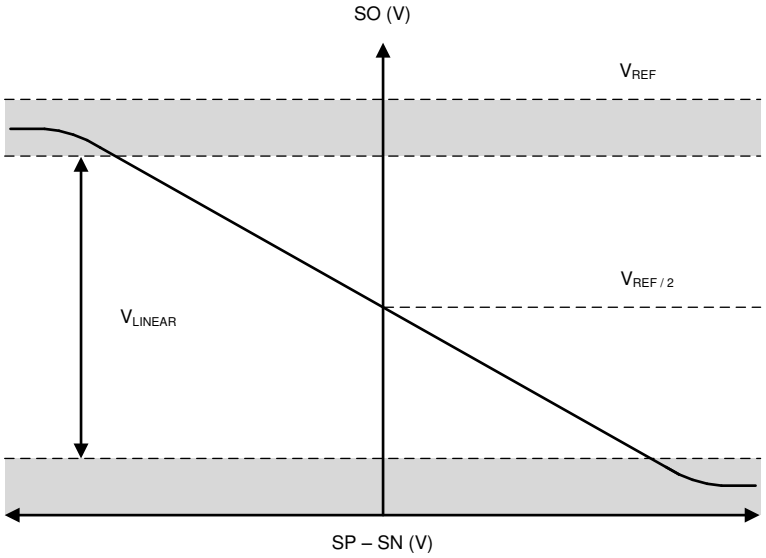


Figure 31. Bidirectional Current-Sense Output

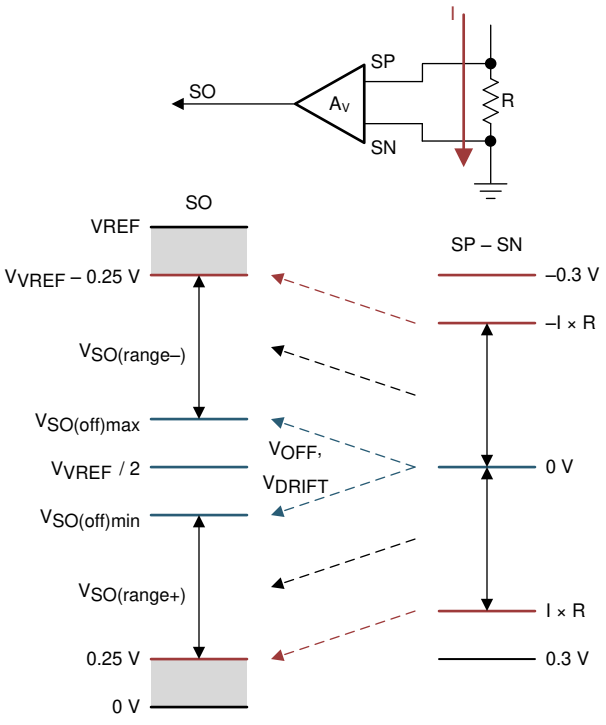


Figure 32. Bidirectional Current Sense Regions

7.3.4.2 Unidirectional Current Sense Operation (SPI only)

On the DRV8304 SPI device, use the VREF_DIV bit to remove the VREF divider. In this case the shunt amplifier operates unidirectionally and the SOx outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). Use Equation 4 to calculate the current through the shunt resistor.

$$I = \frac{\left(\left(V_{VREF} - 0.3\right) - V_{SOX}\right)}{\left(G_{CSA} \times R_{SENSE}\right)} \quad (4)$$

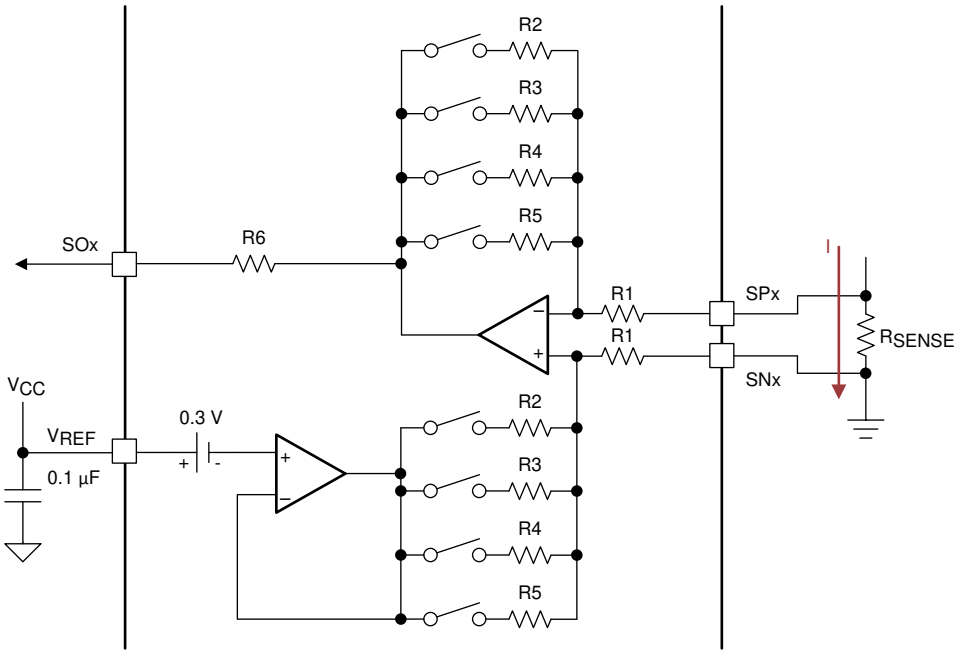


Figure 33. Unidirectional Current-Sense Configuration

Figure 34 and Figure 35 show the detail of the amplifier operational range. In unidirectional operation, the amplifier output for 0-V input is set at VREF – 0.3 V. In this operating mode the amplifier output only responds to a positive current through the shunt resistor. The amplifier has a defined linear region in which it can maintain operation.

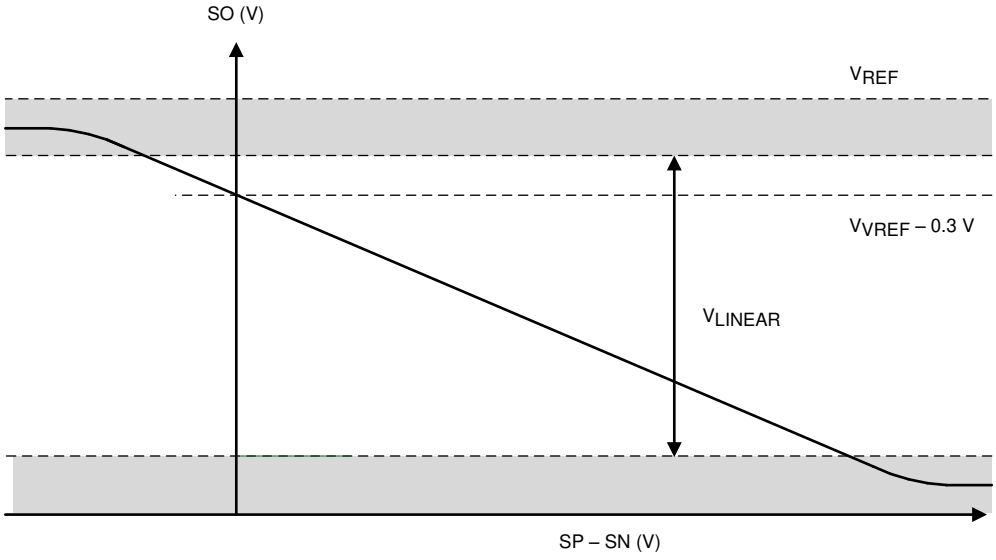


Figure 34. Unidirectional Current-Sense Output

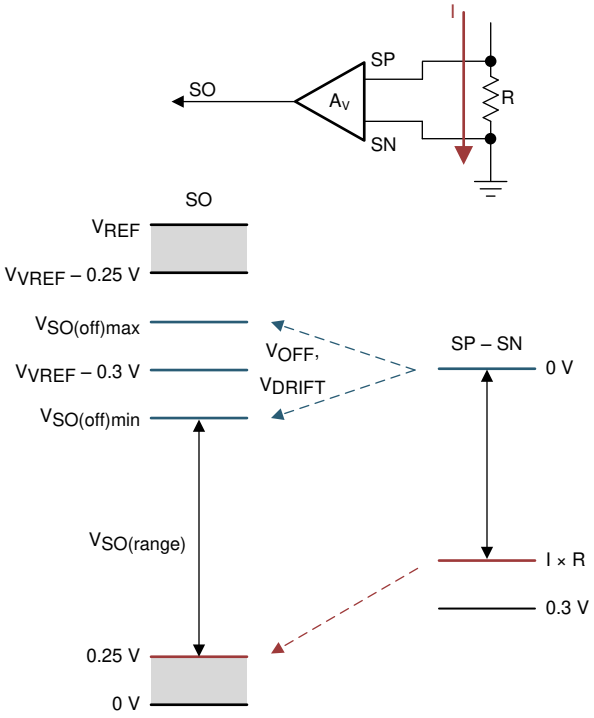


Figure 35. Unidirectional Current-Sense Regions

7.3.4.3 Offset Calibration

The DRV8304 device provides an auto calibration feature to minimize the amplifier input offset on power up or during an ENABLE reset pulse to account for temperature and device variation. Auto calibration is performed on both the hardware and SPI device options. The auto calibration begins immediately after the VREF pin crosses the minimum operational VREF voltage and completes in several µs (max 500 µs). During auto calibration, the inputs to the amplifier are disconnected from SPX and SNX pin and shorted internally. After auto calibration the amplifiers are ready for operation.

For the SPI device option, auto calibration can also be performed during run time by setting the AUTOCAL bit. If the AUTOCAL bit is already set once, then the user must reset the bit and again set it to perform the auto-calibration. The user must wait for at least 500 µs before another write to ensure a successful calibration. The user is recommended not to sample CSA outputs during the AUTOCAL operation.

In addition to this, the device also supports an external calibration through the SPI registers (SPI_CAL) in SPI device or through CAL pin in hardware device variant. When the calibration is enabled (CAL pin or SPI_CAL), the inputs to the amplifier are shorted internally, and the amplifier voltage can be observed though SOX pin for doing the external calibration. For the best results, perform offset calibration when the external MOSFETS are not switching to reduce the potential noise impact to the amplifier. DC calibration can be done at any time, even when the half-bridges are operating. Figure 36 shows a diagram of the calibration mode

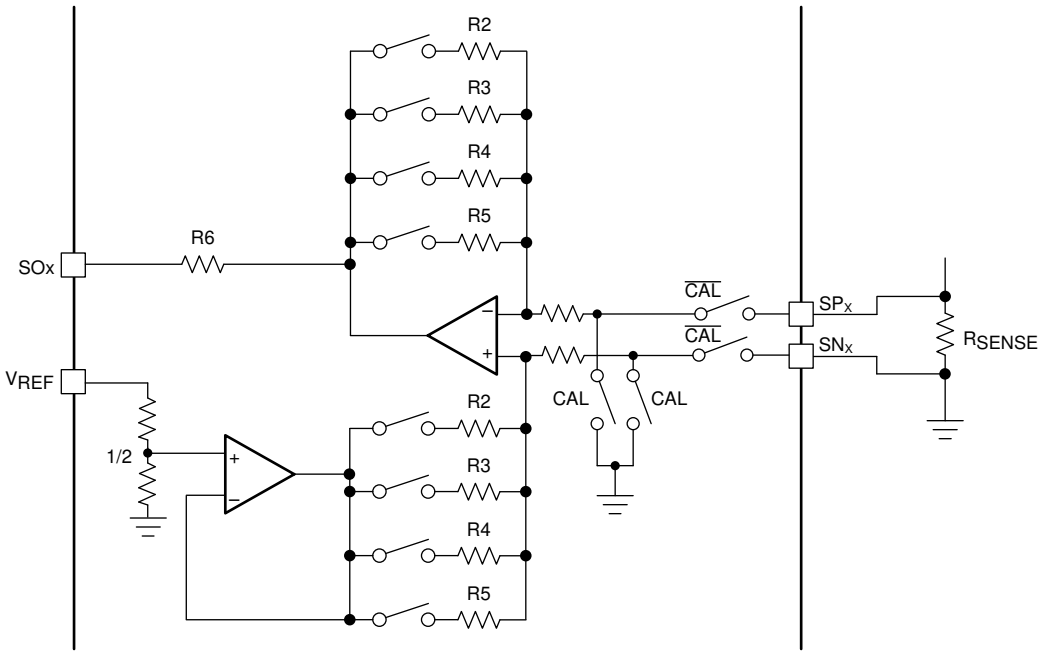


Figure 36. Amplifier Calibration Mode

7.3.5 Gate-Driver Protection Circuits

The DRV8304 device is fully protected against VM undervoltage, charge pump undervoltage, MOSFET V_{DS} overcurrent, gate driver shorts, and overtemperature events.

Table 7. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$V_{VM} < V_{UVLO}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
Charge pump undervoltage (CPUV)	$V_{VCP} < V_{CPUV}$	DIS_CPUV = 0b	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
		DIS_CPUV = 1b	None	Active	Active	
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SEN\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b or DIS_SEN = 1b	None	Active	Active	No action
Gate driver fault (GDF)	Gate voltage stuck > t_{DRIVE}	DIS_GDF = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		DIS_GDF = 1b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$
		OTW_REP = 0b	None	Active	Active	No action
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$

7.3.5.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The FAULT and VM_UVLO bits are also latched high in the registers on the SPI device. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the VM undervoltage condition is removed. The VM_UVLO bit remains set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}).

7.3.5.2 VCP Charge-Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls below the V_{CPUV} threshold voltage of the charge pump, all of the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and CPUV bits are also latched high in the registers on the SPI device. Normal operation resumes (gate-driver operation and the nFAULT pin is released) when the VCP undervoltage condition is removed. The CPUV bit remains set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). Setting the DIS_CPUV bit high on the SPI device disables this protection feature. On the hardware interface device, the CPUV protection is always enabled.

7.3.5.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized and action is taken according to the OCP_MODE. On hardware interface devices, the V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4.5 µs, and the OCP_MODE is configured for 4-ms automatic retry. Moreover, the VDS_OCP can be disabled by tying the VDS pin to DVDD. On SPI devices, the V_{VDS_OCP} threshold is set through the VDS_LVL SPI register, and the OCP_MODE bit can operate in four different modes: V_{DS} latched shutdown, V_{DS} automatic retry, V_{DS} report only, and V_{DS} disabled.

7.3.5.3.1 V_{DS} Latched Shutdown (OCP_MODE = 00b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

7.3.5.3.2 V_{DS} Automatic Retry (OCP_MODE = 01b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, VDS_OCP, and MOSFET OCP bits remain latched until the t_{RETRY} period expires.

7.3.5.3.3 V_{DS} Report Only (OCP_MODE = 10b)

No protective action occurs after a VDS_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, VDS_OCP, and corresponding MOSFET OCP bits high in the SPI registers. The gate drivers continue to operate normally. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the VDS_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

7.3.5.3.4 V_{DS} Disabled (OCP_MODE = 11b)

No action occurs after a VDS_OCP event in this mode.

7.3.5.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Half-bridge overcurrent is also monitored by sensing the voltage drop across the external current-sense resistor with the SPX pin. If at any time, the voltage on the SP input of the current-sense amplifier exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized and action is done according to the OCP_MODE bit. On the hardware interface device, the V_{SENSE} threshold is fixed at 1 V, t_{OCP_DEG} is fixed at 4 µs, and the OCP_MODE bit for V_{SENSE} is fixed for 4-ms automatic retry. On the SPI device, the V_{SENSE} threshold is set through the SEN_LVL SPI register and the OCP_MODE bit can operate in four different modes: V_{SENSE} latched shutdown, V_{SENSE} automatic retry, V_{SENSE} report only, and V_{SENSE} disabled.

7.3.5.4.1 V_{SENSE} Latched Shutdown (OCP_MODE = 00b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and SEN_OCP bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

7.3.5.4.2 V_{SENSE} Automatic Retry (OCP_MODE = 01b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, SEN_OCP, and corresponding sense OCP bits are latched high in the SPI registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, SEN_OCP, and sense OCP bits remain latched until the t_{RETRY} period expires.

7.3.5.4.3 V_{SENSE} Report Only (OCP_MODE = 10b)

No protective action occurs after a SEN_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT and SEN_OCP bits high in the SPI registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT released) when the SEN_OCP condition is removed and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

7.3.5.4.4 V_{SENSE} Disabled (OCP_MODE = 11b or DIS_SEN = 1b)

No action occurs after a SEN_OCP event in this mode. The SEN_OCP bit can be disabled independently of the VDS_OCP bit by using the DIS_SEN SPI register.

7.3.5.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault might be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault might be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin is driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the gate-driver fault condition is removed and a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). On the SPI device, setting the DIS_GDF_UVLO bit high disables this protection feature.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve a gate driver fault in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

7.3.5.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of the SPI device. The device performs no additional action and continues to function. When the die temperature decreases below the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin by setting the OTW_REP bit to 1b through the SPI registers.

7.3.5.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and TSD bits are latched high. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the overtemperature condition is removed. The TSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This protection feature cannot be disabled.

7.4 Device Functional Modes

7.4.1 Gate Driver Functional Modes

7.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV8304 device. When the ENABLE pin is low, the device enters a low-power sleep mode. In sleep mode, all gate drivers are disabled, all external MOSFETs are disabled, the charge pump is disabled, the DVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device enters sleep mode. The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal resistor.

NOTE

During power up and power down of the device through the ENABLE pin, the nFAULT pin is held low as the internal regulators enable or disable. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

7.4.1.2 Operating Mode

When the ENABLE pin is high and $V_{VM} > V_{UVLO}$, the device enters operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, DVDD regulator, and SPI bus are active and hardware inputs are latched.

NOTE

If the ENABLE pin is left floating, the device will be in Operating Mode.

7.4.1.3 Fault Reset (CLR_FLT or ENABLE Reset Pulse)

In the case of device latched faults, the DRV8304 device enters a partial shutdown state to help protect the external power MOSFETs and system.

When the fault condition has been removed the device can reenter the operating state by either setting the CLR_FLT SPI bit on the SPI device or issuing a result pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will begin the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks

7.5 Programming

This section applies only to the DRV8304 SPI device.

7.5.1 SPI Communication

7.5.1.1 SPI

On the DRV8304 SPI device, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16-bit word, with a 5-bit command and 11 bits of data. The SPI output data (SDO) word consists of 11-bit register data. The first 5 bits are don't care bits.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is

Programming (continued)

placed in the Hi-Z state.

- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for the transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 5-bit command data.

7.5.1.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 4 address bits, A (bits B14 through B11)
- 11 data bits, D (bits B11 through B0)

The SDO output data word is 16 bits long and the first 5 bits are don't care bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 8. SDI Input Data Word Format

R/W	ADDRESS				DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 9. SDO Output Data Word Format

DON'T CARE BITS					DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

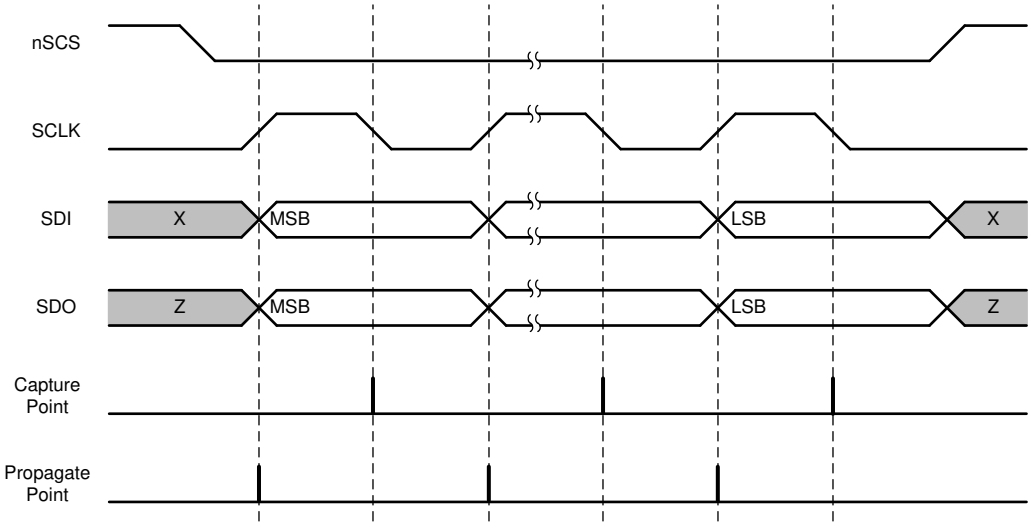


Figure 37. SPI Slave Timing Diagram

7.6 Register Maps

This section applies only to the DRV8304 SPI device.

NOTE

Do not modify reserved registers or addresses not listed in the register map (Table 10). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0. To help prevent erroneous SPI writes from the master controller, set the LOCK bits to lock the SPI registers.

Table 10. DRV8304S Register Map

Name	10	9	8	7	6	5	4	3	2	1	0	Type	Address
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	Reserved	DIS_CPUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			Reserved	IDRIVEP_HS			Reserved	IDRIVEN_HS			RW	3h
Gate Drive LS	CBC	TDRIVE		Reserved	IDRIVEP_LS			Reserved	IDRIVEN_LS			RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_ACT	Reserved		VDS_LVL			RW	5h
CSA Control	Reserved	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	SPI_CAL	AUTOCAL	Reserved	SEN_LVL		RW	6h
Reserved	Reserved											RW	7h

7.6.1 Status Registers (DRV8304S Only)

The status registers are used to reporting warning and fault conditions. The status registers are read-only registers

Complex bit access types are encoded to fit into small table cells. Table 11 shows the codes that are used for access types in this section.

Table 11. Status Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 Fault Status Register 1 (Address = 0x00) [reset = 0x00]

The fault status register 1 is shown in Figure 38 and described in Table 12.

Register access type: Read only

Figure 38. Fault Status Register 1

10	9	8	7	6	5	4	3	2	1	0
FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 12. Fault Status Register 1 Field Descriptions

Bit	Field	Type	Default	Description
10	FAULT	R	0b	Logic OR of FAULT status registers. Mirrors nFAULT pin.
9	VDS_OCP	R	0b	Indicates VDS monitor overcurrent fault condition
8	GDF	R	0b	Indicates gate drive fault condition
7	UVLO	R	0b	Indicates undervoltage lockout fault condition
6	OTSD	R	0b	Indicates overtemperature shutdown
5	VDS_HA	R	0b	Indicates VDS overcurrent fault on the A high-side MOSFET
4	VDS_LA	R	0b	Indicates VDS overcurrent fault on the A low-side MOSFET
3	VDS_HB	R	0b	Indicates VDS overcurrent fault on the B high-side MOSFET
2	VDS_LB	R	0b	Indicates VDS overcurrent fault on the B low-side MOSFET
1	VDS_HC	R	0b	Indicates VDS overcurrent fault on the C high-side MOSFET
0	VDS_LC	R	0b	Indicates VDS overcurrent fault on the C low-side MOSFET

7.6.1.2 Fault Status Register 2 (Address = 0x01) [reset = 0x00]

The fault status register 2 is shown in Figure 39 and described in Table 13.

Register access type: Read only

Figure 39. Fault Status Register 2

10	9	8	7	6	5	4	3	2	1	0
SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 13. Fault Status Register 2 Field Descriptions

Bit	Field	Type	Default	Description
10	SA_OC	R	0b	Indicates overcurrent on phase A sense amplifier (DRV8304S)
9	SB_OC	R	0b	Indicates overcurrent on phase B sense amplifier (DRV8304S)
8	SC_OC	R	0b	Indicates overcurrent on phase C sense amplifier (DRV8304S)
7	OTW	R	0b	Indicates overtemperature warning
6	CPUV	R	0b	Indicates charge pump undervoltage fault condition
5	VGS_HA	R	0b	Indicates gate drive fault on the A high-side MOSFET
4	VGS_LA	R	0b	Indicates gate drive fault on the A low-side MOSFET
3	VGS_HB	R	0b	Indicates gate drive fault on the B high-side MOSFET
2	VGS_LB	R	0b	Indicates gate drive fault on the B low-side MOSFET
1	VGS_HC	R	0b	Indicates gate drive fault on the C high-side MOSFET
0	VGS_LC	R	0b	Indicates gate drive fault on the C low-side MOSFET

7.6.2 Control Registers (DRV8304S Only)

The control registers are used to configure the device. The control registers are read and write capable

Complex bit access types are encoded to fit into small table cells. Table 14 shows the codes that are used for access types in this section.

Table 14. Control Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1 Driver Control Register (Address = 0x02) [reset = 0x00]

The driver control register is shown in Figure 40 and described in Table 15.

Register access type: Read/Write

Figure 40. Driver Control Register

10	9	8	7	6	5	4	3	2	1	0
Reserved	DIS _CPUV	DIS _GDF	OTW _REP	PWM_MODE		1PWM _COM	1PWM _DIR	COAST	BRAKE	CLR _FLT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 15. Driver Control Field Descriptions

Bit	Field	Type	Default	Description
10	Reserved	R/W	0b	Reserved
9	DIS_CPUV	R/W	0b	**0b = Charge-pump undervoltage lockout fault is enabled** 1b = Charge-pump undervoltage lockout fault is disabled
8	DIS_GDF	R/W	0b	**0b = Gate drive fault is enabled** 1b = Gate drive fault is disabled
7	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
6-5	PWM_MODE	R/W	00b	**00b = 6x PWM Mode** 01b = 3x PWM mode 10b = 1x PWM mode 11b = Independent PWM mode
4	1PWM_COM	R/W	0b	**0b = 1x PWM mode uses synchronous rectification** 1b = 1x PWM mode uses asynchronous rectification (diode freewheeling)
3	1PWM_DIR	R/W	0b	In 1x PWM mode this bit is ORed with the INHC (DIR) input
2	COAST	R/W	0b	Write a 1b to this bit to put all MOSFETs in the Hi-Z state
1	BRAKE	R/W	0b	Write a 1b to this bit to turn on all three low-side MOSFETs in 1x PWM mode. This bit is ORed with the INLC (BRAKE) input.
0	CLR_FLT	R/W	0b	Write a 1b to this bit to clear latched fault bits. This bit automatically resets after being written.

7.6.2.2 Gate Drive HS Register (Address = 0x03) [reset = 0x377]

The gate drive HS register is shown in Figure 41 and described in Table 16.

Register access type: Read/Write

Figure 41. Gate Drive HS Register

10	9	8	7	6	5	4	3	2	1	0
LOCK			Reserved	IDRIVEP_HS			Reserved	IDRIVEN_HS		
R/W-011b			R/W-0b	R/W-111b			R/W-0b	R/W-111b		

Table 16. Gate Drive HS Field Descriptions

Bit	Field	Type	Default	Description
10-8	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x02h bits 0-2. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
7	Reserved	R/W	0b	Reserved
6-4	IDRIVEP_HS	R/W	111b	000b = 15 mA 001b = 15 mA 010b = 45 mA 011b = 60 mA 100b = 90 mA 101b = 105 mA 110b = 135 mA **111b = 150 mA**
3	Reserved	R/W	0b	Reserved
2-0	IDRIVEN_HS	R/W	111b	000b = 30 mA 001b = 30 mA 010b = 90 mA 011b = 120 mA 100b = 180 mA 101b = 210 mA 110b = 270 mA **111b = 300 mA**

7.6.2.3 Gate Drive LS Register (Address = 0x04) [reset = 0x777]

The gate drive LS register is shown in Figure 42 and described in Table 17.

Register access type: Read/Write

Figure 42. Gate Drive LS Register

10	9	8	7	6	5	4	3	2	1	0
CBC	TDRIVE		Reserved	IDRIVEP_LS			Reserved	IDRIVEN_LS		
R/W-1b	R/W-11b		R/W-0b	R/W-111b			R/W-0b	R/W-111b		

Table 17. Gate Drive LS Register Field Descriptions

Bit	Field	Type	Default	Description
10	CBC	R/W	1b	In retry OCP_MODE, for both VDS_OCP and SEN_OCP, the fault is automatically cleared when a PWM input is given
9-8	TDRIVE	R/W	11b	00b = 500-ns peak gate-current drive time 01b = 1000-ns peak gate-current drive time 10b = 2000-ns peak gate-current drive time **11b = 4000-ns peak gate-current drive time**
7	Reserved	R/W	0b	Reserved
6-4	IDRIVEP_LS	R/W	111b	000b = 15 mA 001b = 15 mA 010b = 45 mA 011b = 60 mA 100b = 90 mA 101b = 105 mA 110b = 135 mA **111b = 150 mA**
3	Reserved	R/W	0b	Reserved
2-0	IDRIVEN_LS	R/W	111b	000b = 30 mA 001b = 30 mA 010b = 90 mA 011b = 120 mA 100b = 180 mA 101b = 210 mA 110b = 270 mA **111b = 300 mA**

7.6.2.4 OCP Control Register (Address = 0x05) [reset = 0x145]

The OCP control register is shown in Figure 43 and described in Table 18.

Register access type: Read/Write

Figure 43. OCP Control Register

10	9	8	7	6	5	4	3	2	1	0
TRETRY	DEAD_TIME		OCP_MODE		OCP_ACT	Reserved		VDS_LVL		
R/W-0b	R/W-01b		R/W-01b		R/W-0b	R/W-00b		R/W-101b		

Table 18. OCP Control Field Descriptions

Bit	Field	Type	Default	Description
10	TRETRY	R/W	0b	**0b = VDS_OCP and SEN_OCP retry time is 4 ms** 1b = VDS_OCP and SEN_OCP retry time is 50 µs
9-8	DEAD_TIME	R/W	01b	00b = 50-ns dead time **01b = 100-ns dead time** 10b = 200-ns dead time 11b = 400-ns dead time
7-6	OCP_MODE	R/W	01b	00b = Overcurrent causes a latched fault **01b = Overcurrent causes an automatic retrying fault** 10b = Overcurrent is report only but no action is taken 11b = Overcurrent is not reported and no action is taken
5	OCP_ACT	R/W	0b	**0b = All three half-bridges are shutdown in response to VDS_OCP and SEN_OCP** 1b = Associated half-bridge is shutdown in response to VDS_OCP and SEN_OCP
4-3	Reserved	R/W	00b	Reserved
2-0	VDS_LVL	R/W	101b	000b = 0.15 V 001b = 0.24 V 010b = 0.40V 011b = 0.51 V 100b = 0.60 V **101b = 0.90 V** 110b = 1.8 V 111b = VDS Disabled

7.6.2.5 CSA Control Register (Address = 0x06) [reset = 0x283]

The CSA control register is shown in Figure 44 and described in Table 19.

Register access type: Read/Write

Figure 44. CSA Control Register

10	9	8	7	6	5	4	3	2	1	0
Reserved	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	SPI_CAL	AUTO CAL	Reserved	SEN_LVL	
R/W-0b	R/W-1b	R/W-0b	R/W-10b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Table 19. CSA Control Field Descriptions

Bit	Field	Type	Default	Description
10	Reserved	R/W	0b	Reserved
9	VREF_DIV	R/W	1b	0b = Sense amplifier reference voltage is VREF (unidirectional mode) **1b = Sense amplifier reference voltage is VREF divided by 2**
8	LS_REF	R/W	0b	**0b = VDS_OCP for the low-side MOSFET is measured across SHx to SPx** 1b = VDS_OCP for the low-side MOSFET is measured across SHx to SNx
7-6	CSA_GAIN	R/W	10b	00b = 5-V/V shunt amplifier gain 01b = 10-V/V shunt amplifier gain **10b = 20-V/V shunt amplifier gain** 11b = 40-V/V shunt amplifier gain
5	DIS_SEN	R/W	0b	**0b = Sense overcurrent fault is enabled** 1b = Sense overcurrent fault is disabled
4	SPI_CAL	R/W	0b	**0b = Disable sense amplifier CAL function** 1b = Enable sense amplifier CAL function
3	AUTOCAL	R/W	0b	**0b = AUTOCAL operation remains disabled in run mode** 1b = Perform AUTOCAL operation
2	Reserved	R/W	0b	Reserved
1-0	SEN_LVL	R/W	11b	00b = Sense OCP 0.25 V 01b = Sense OCP 0.5 V 10b = Sense OCP 0.75 V **11b = Sense OCP 1 V**

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8304 device is primarily used in 3-phase brushless DC motor control applications. The design procedures in the *Typical Application* section highlight how to use and configure the DRV8304 device.

8.2 Typical Application

8.2.1 Primary Application

In this application the amplifiers are configured to sense bi-directional currents in each of the three half-bridge legs.

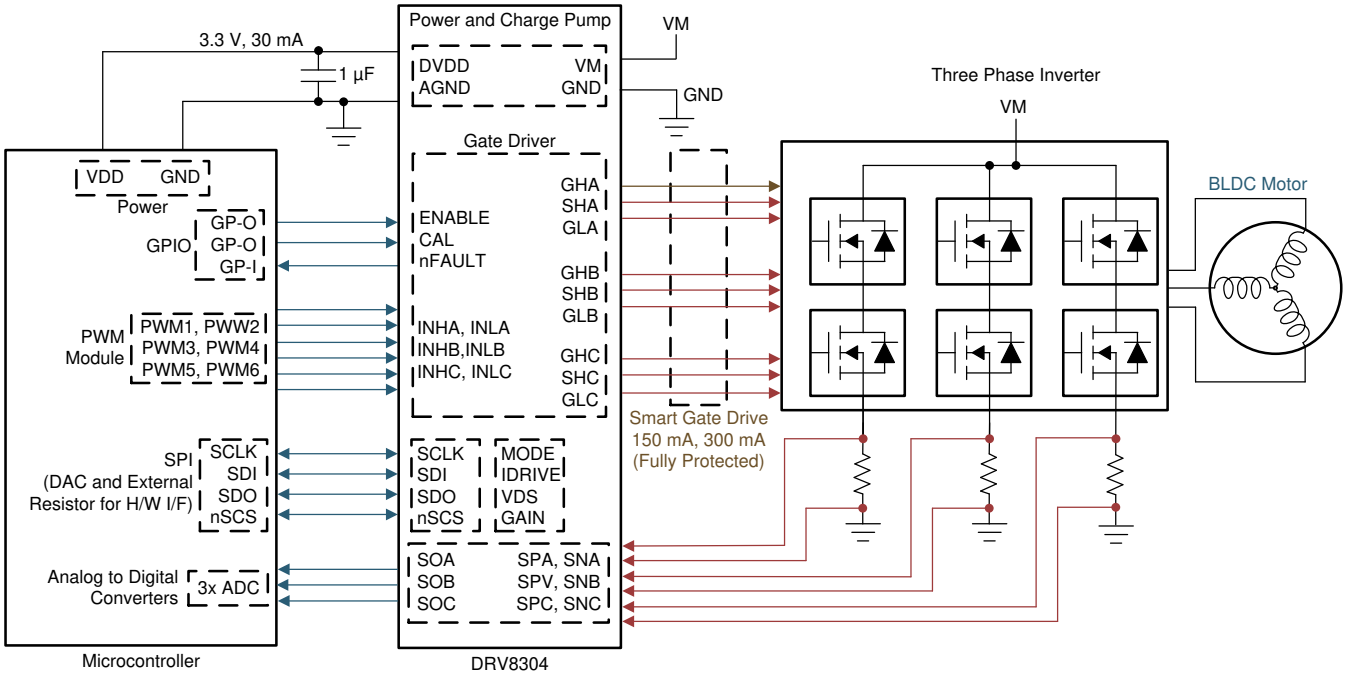


Figure 45. Primary Application Schematic

Typical Application (continued)

8.2.1.1 Design Requirements

Table 20 lists the example input parameters for the system design.

Table 20. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	24 V
Supply voltage range		8 V to 38 V
MOSFET part number		CSD18514Q5A
MOSFET total gate charge	Q_g	29 nC (typical) at V_{VGS} = 10 V
MOSFET gate to drain charge	Q_{gd}	5 nC (typical)
Target output rise time	t_r	100 to 300 ns
Target output fall time	t_f	50 to 150 ns
PWM frequency	f_{PWM}	45 kHz
Maximum motor current	I_{max}	50 A
Winding sense current range	I_{SENSE}	–20 A to +20 A
Motor RMS current	I_{RMS}	14.14 A
Sense resistor power rating	P_{SENSE}	2 W
System ambient temperature	T_A	–20°C to +105°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External MOSFET Support

The DRV8304 MOSFET support is based on the charge-pump capacity and output PWM switching frequency. For a quick calculation of MOSFET driving capacity, use Equation 5 and Equation 6 for three phase BLDC motor applications.

Trapezoidal 120° Commutation: $I_{VCP} > Q_g \times f_{PWM}$ (5)

Sinusoidal 180° Commutation: $I_{VCP} > 3 \times Q_g \times f_{PWM}$

where

- f_{PWM} is the maximum desired PWM switching frequency.
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage.
- The multiplier based on the commutation control method, may vary based on implementation. (6)

8.2.1.2.1.1 Example

If a system at V_{VM} = 8 V (I_{VCP} = 15 mA) uses a maximum PWM switching frequency of 45 kHz, then the charge pump can support MOSFETs using trapezoidal commutation with a Q_g < 333 nC, and MOSFETs with sinusoidal commutation Q_g < 111 nC. When the VM voltage (V_{VM}) is 8 V, the maximum DRV8304 gate-drive voltage (V_{GSH}) is 7.3 V. Therefore, at 7.3-V gate drive, the target FET (part number CSD18514Q5A) only has a gate charge of approximately 22 nC. Therefore, with this FET, the system can have an adequate margin.

8.2.1.2.2 IDRIVE Configuration

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses. TI recommends adjusting these values in system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are independently adjustable on the SPI device through the SPI registers. On hardware interface devices, both source and sink settings are selected simultaneously on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge (Q_{gd}), desired rise time (t_r), and a desired fall time (t_f), use Equation 7 and Equation 8 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} > \frac{Q_{gd}}{t_r} \quad (7)$$

$$I_{DRIVEN} > \frac{Q_{gd}}{t_f} \quad (8)$$

8.2.1.2.2.1 Example

Use Equation 9 and Equation 10 to calculate the value of $I_{DRIVEP1}$ and $I_{DRIVEP2}$ (respectively) for a gate to drain charge of 5 nC and a rise time from 100 to 300 ns.

$$I_{DRIVEP1} = \frac{5\text{ nC}}{100\text{ ns}} = 50\text{ mA} \quad (9)$$

$$I_{DRIVEP2} = \frac{5\text{ nC}}{300\text{ ns}} = 16.67\text{ mA} \quad (10)$$

Select a value for I_{DRIVEP} that is between 16.67 mA and 50 mA. For this example, the value of I_{DRIVEP} was selected as 45-mA source.

Use Equation 11 and Equation 12 to calculate the value of $I_{DRIVEN1}$ and $I_{DRIVEN2}$ (respectively) for a gate to drain charge of 5 nC and a fall time from 50 to 150 ns.

$$I_{DRIVEN1} = \frac{5\text{ nC}}{50\text{ ns}} = 100\text{ mA} \quad (11)$$

$$I_{DRIVEN2} = \frac{5\text{ nC}}{150\text{ ns}} = 33.33\text{ mA} \quad (12)$$

Select a value for I_{DRIVEN} that is between 33.33 mA and 100 mA. For this example, the value of I_{DRIVEN} was selected as 90-mA sink.

8.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in Equation 13.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \quad (13)$$

8.2.1.2.3.1 Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 50 A. According to the *CSD18514Q5A 40 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 1.8 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10 V is 4.9 mΩ. From these values, the approximate worst-case value of $R_{DS(on)}$ is 1.8 × 4.9 mΩ = 8.82 mΩ.

Using Equation 13 with a value of 8.82 mΩ for $R_{DS(on)}$ and a worst-case motor current of 50 A, Equation 14 shows the calculated the value of the V_{DS} monitors.

$$V_{DS\_OCP} > 50\text{ A} \times 8.82\text{ m}\Omega$$

$$V_{DS\_OCP} > 0.441\text{ V} \quad (14)$$

For this example, the value of V_{DS_OCP} was selected as 0.51 V.

The deglitch time for the V_{DS} overcurrent monitor is fixed at 4.5 µs.

8.2.1.2.4 Sense-Amplifier Bidirectional Configuration

The sense-amplifier gain and the sense-resistor value on the DRV8304 device are selected based on the target current range, VREF voltage supply, sense-resistor power rating, and operating temperature range. In bidirectional operation of the sense amplifier, the dynamic range at the output is approximately calculated as shown in Equation 15.

$$V_O = \left(V_{VREF} - 0.25\text{ V}\right) - \frac{V_{VREF}}{2} \quad (15)$$

Use Equation 16 to calculate the approximate value of the selected sense resistor with V_O calculated using Equation 15.

$$R = \frac{V_O}{A_V \times I} \quad P_{SENSE} > I_{RMS}^2 \times R \tag{16}$$

From Equation 15 and Equation 16, select a target gain setting based on the power rating of the target-sense resistor.

8.2.1.2.4.1 Example

In this system example, the value of the VREF voltage is 3.3 V with a sense current from –20 to +20 A. The linear range of the SOx output is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = (3.3\text{ V} - 0.25\text{ V}) - \frac{3.3\text{ V}}{2} = 1.4\text{ V} \tag{17}$$

$$R = \frac{1.4\text{ V}}{A_V \times 20\text{ A}} \quad 2\text{ W} > 14.14^2 \times R \rightarrow R < 10\text{ m}\Omega \tag{18}$$

$$10\text{ m}\Omega > \frac{1.4\text{ V}}{A_V \times 20\text{ A}} \rightarrow A_V > 7 \tag{19}$$

Therefore, the gain setting must be selected as 10 V/V or 20 V/V and the value of the sense resistor must be less than 10 mΩ to meet the power requirement for the sense resistor. For this example, the gain setting was selected as 10 V/V. The value of the resistor and worst case current can be verified that R < 10 mΩ and I_{max} = 20 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

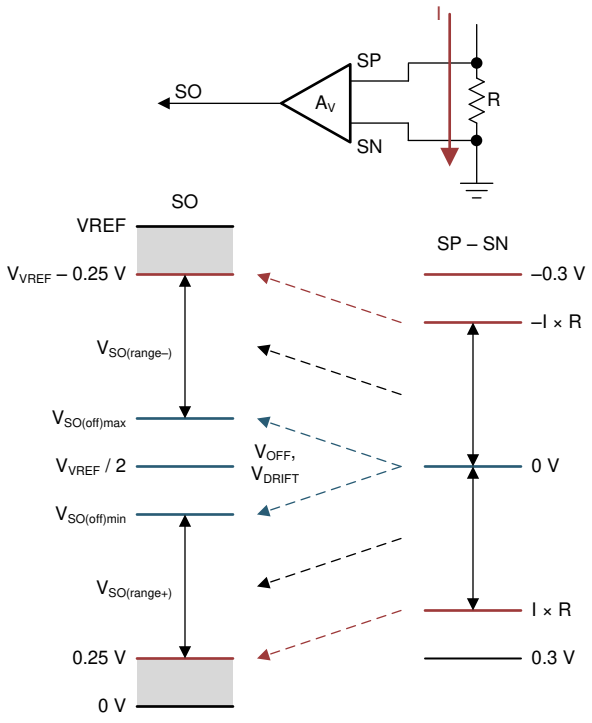


Figure 46. Sense Amplifier Configuration

8.2.1.3 Application Curves

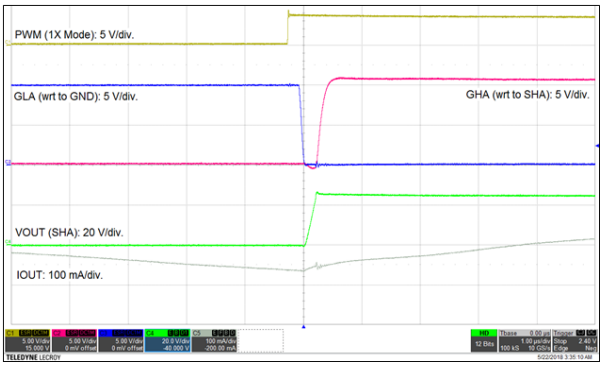


Figure 47. IDRIVE Maximum Setting

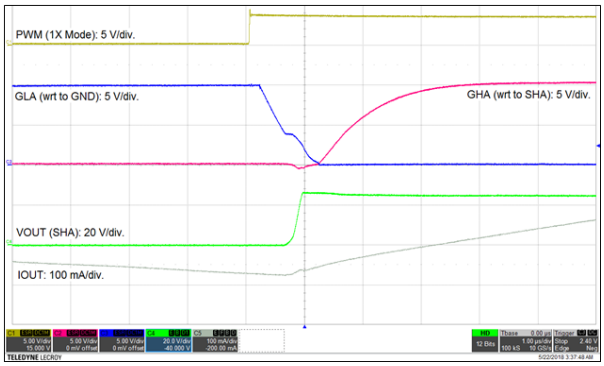


Figure 48. IDRIVE Minimum Setting

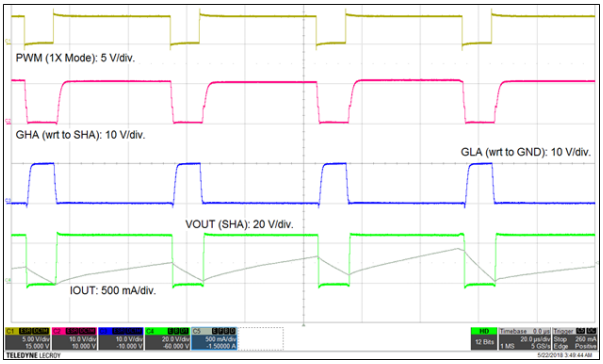


Figure 49. Gate Drive 80% Duty Cycle

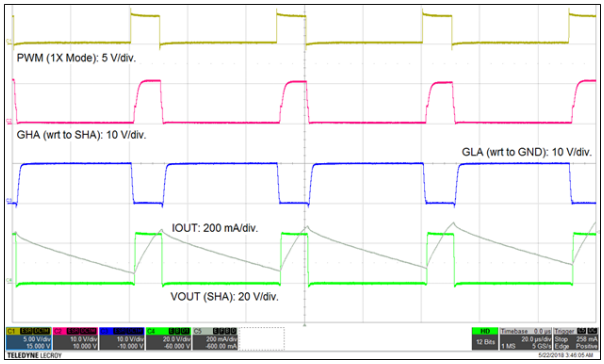


Figure 50. Gate Drive 20% Duty Cycle

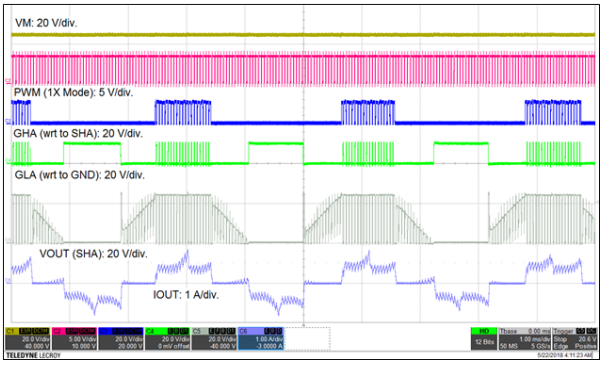


Figure 51. Motor Operation at 80% PWM Duty

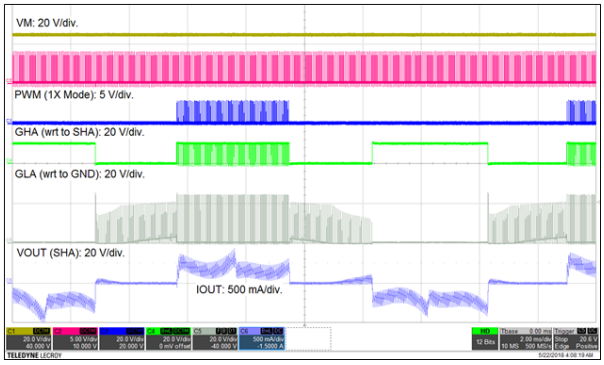


Figure 52. Motor Operation at 20% PWM Duty

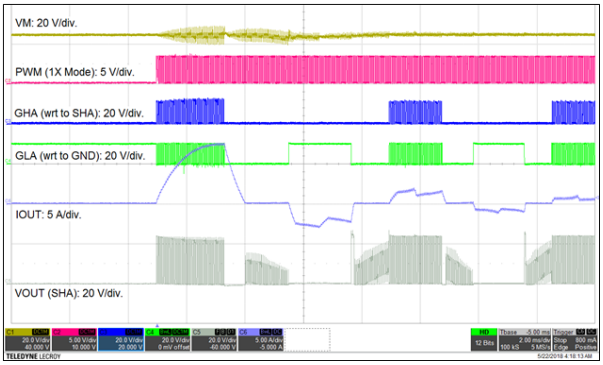


Figure 53. Motor Starting With PWM Duty Change

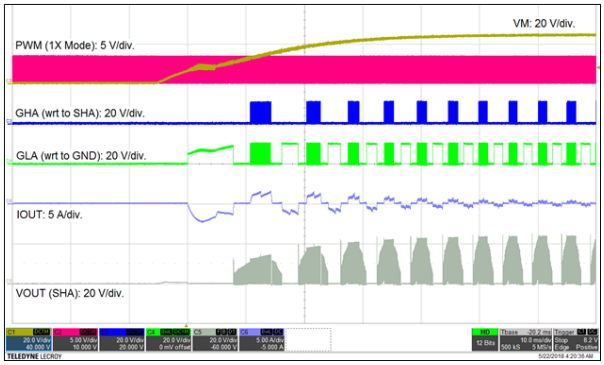


Figure 54. Motor Starting With Supply Voltage Change

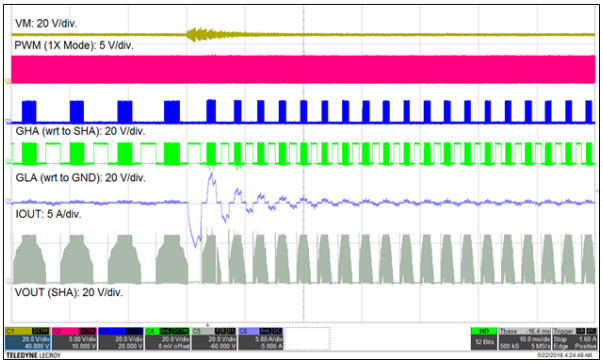


Figure 55. Motor Performance at Speed Change

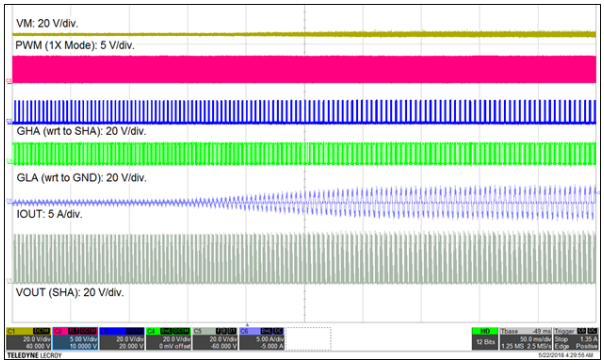


Figure 56. Motor Performance at Load Change

8.2.2 Alternative Application

In this application, a single-sense amplifier is used in unidirectional mode for a summing current-sense scheme often used in trapezoidal or hall-based BLDC commutation control.

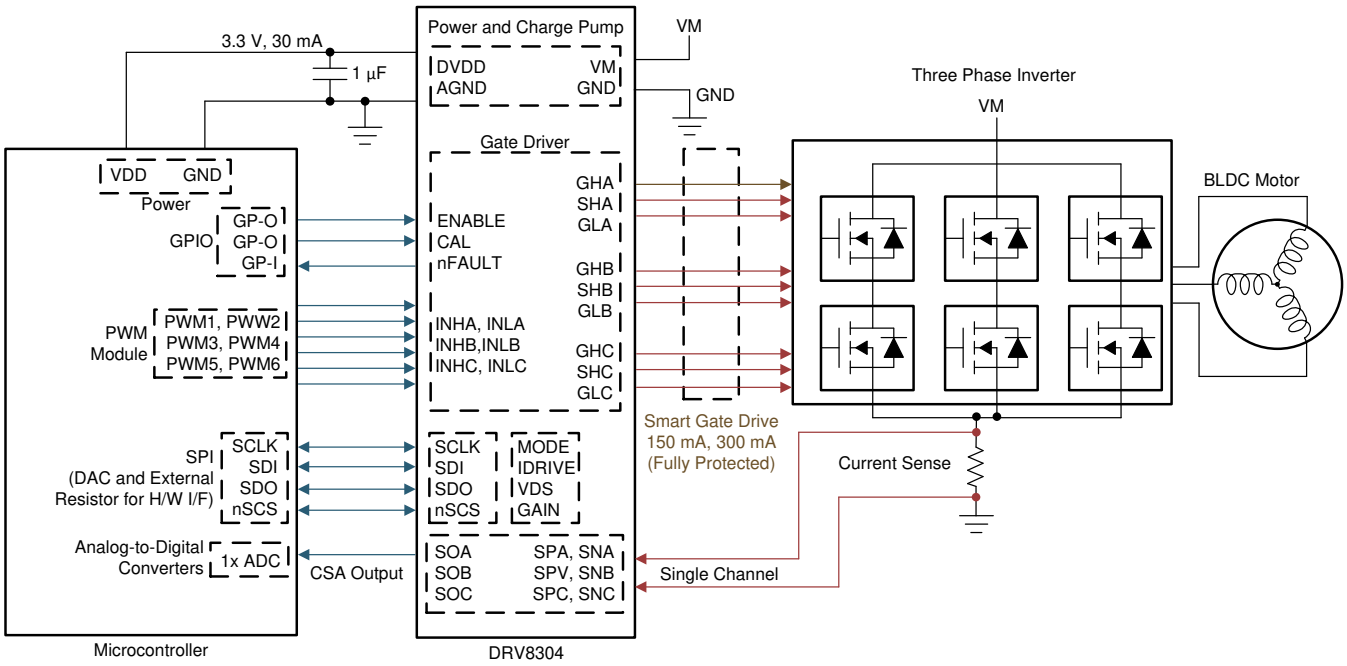


Figure 57. Alternative Application Schematic

8.2.2.1 Design Requirements

Table 21 lists the example design input parameters for system design.

Table 21. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
ADC reference voltage	V_{VREF}	3.3 V
Sensed current	I_{SENSE}	0 to 20 A
Motor RMS current	I_{RMS}	14.14 A
Sense-resistor power rating	P_{SENSE}	3 W
System ambient temperature	T_A	–20°C to +125°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Sense-Amplifier Unidirectional Configuration

The sense amplifiers are configured to be unidirectional through the registers on the SPI device by writing a 0b to the VREF_DIV bit.

The sense-amplifier gain and sense resistor values are selected based on the target current range, VREF, sense-resistor power rating, and operating temperature range. In unidirectional operation of the sense amplifier, use Equation 20 to calculate the approximate value of the dynamic range at the output.

$$V_O = \left(V_{VREF} - 0.25\ V\right) - 0.25\ V = V_{VREF} - 0.5\ V \quad (20)$$

Use Equation 21 to calculate the approximate value of the selected sense resistor.

$$R = \frac{V_O}{A_V \times I} \qquad P_{SENSE} > I_{RMS}^2 \times R$$

where

- $V_O = V_{VREF} - 0.5\ V$ (21)

From Equation 20 and Equation 21, select a target gain setting based on the power rating of a target sense resistor.

8.2.2.2.1.1 Example

In this system example, the value of VREF is 3.3 V with a sense current from 0 to 40 A. The linear range of the SOx output for the DRV8304 device is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense-amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = 3.3\ V - 0.5\ V = 2.8\ V \quad (22)$$

$$R = \frac{2.8\ V}{A_V \times 20\ A} \quad 3\ W > 14.14^2 \times R \rightarrow R < 15\ m\Omega \quad (23)$$

$$15\ m\Omega > \frac{2.8\ V}{A_V \times 20\ A} \rightarrow A_V > 9.3 \quad (24)$$

Therefore, the gain setting must be selected as 10 V/V or 20 V/V and the value of the sense resistor must be less than 15 mΩ to meet the power requirement for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst-case current can be verified that R < 15 mΩ and I_{max} = 20 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

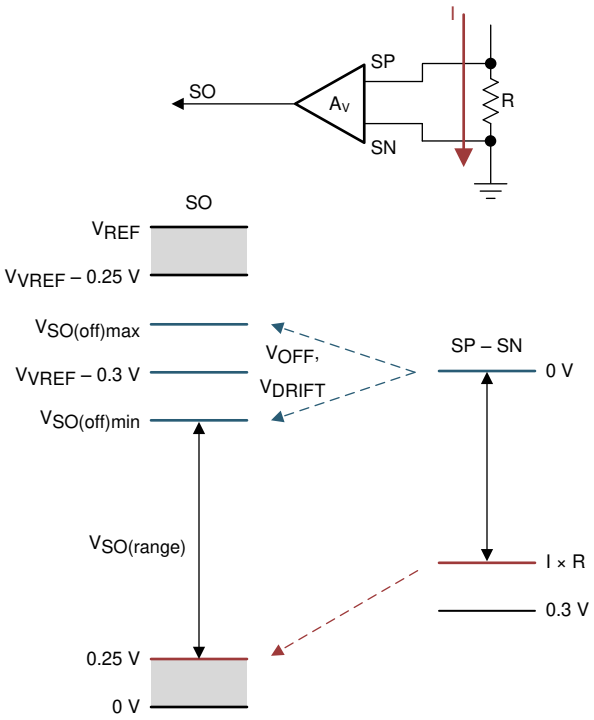


Figure 58. Sense Amplifier Configuration

9 Power Supply Recommendations

The DRV8304 device is designed to operate from an input voltage supply (VM) range from 6 V to 38 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

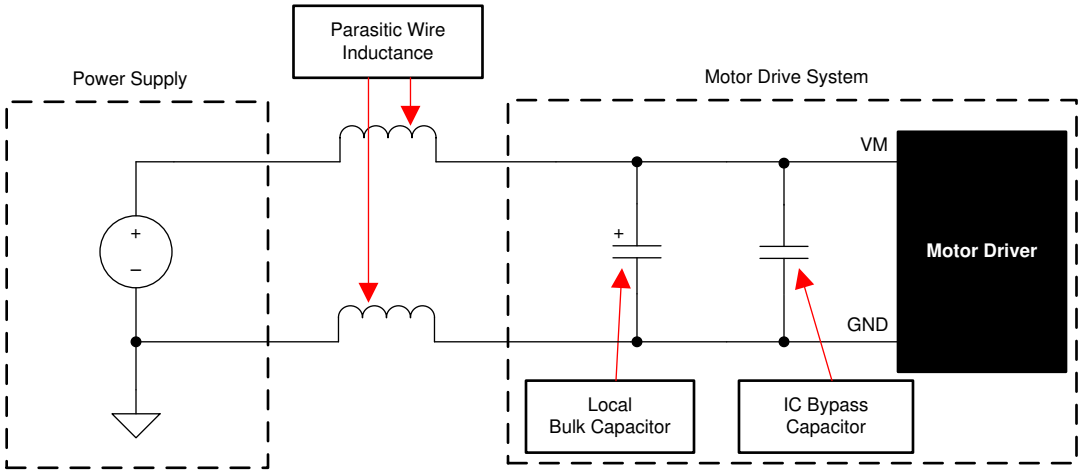


Figure 59. Motor Drive Supply Parasitics Example

10 Layout

10.1 Layout Guidelines

Bypass the VM pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 22 nF, rated for VM, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

The VDRAIN pin can be shorted directly to the VM pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SNx pins directly to the PGND pin. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations allow for more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

10.2 Layout Example

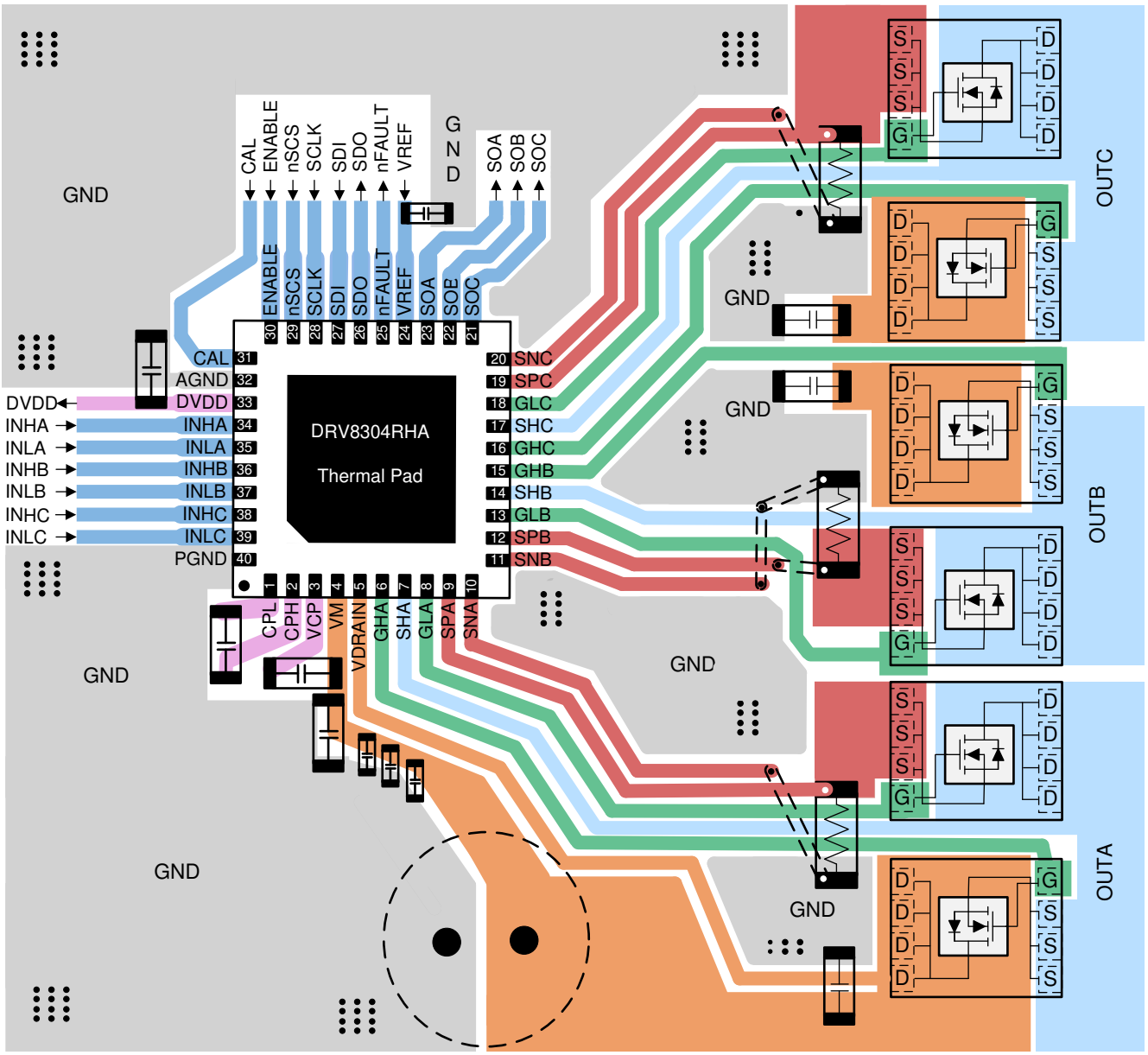


Figure 60. Layout Example

11 Device and Documentation Support

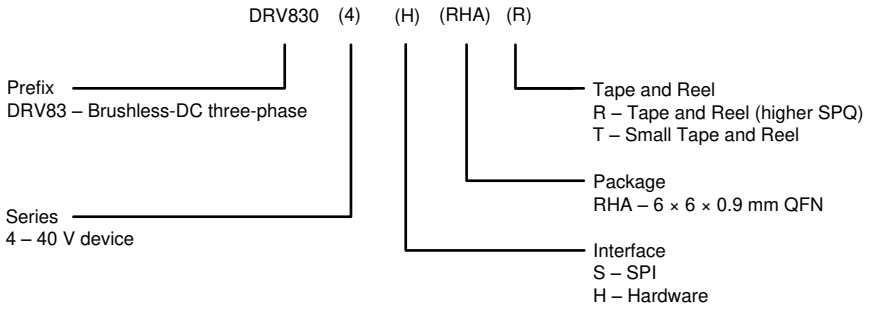
11.1 Device Support

Refer to the TI Design for development support:

10.8-V/30-W, >95% Efficiency, 4.3-cm2, Power Stage Reference Design for Brushless DC Servo Drive TI Design

11.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:



11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *BOOSTXL-DRV8304H EVM User's Guide* user's guide
- Texas Instruments, *BOOSTXL-DRV8304x EVM GUI User's Guide* user's guide
- Texas Instruments, *BOOSTXL-DRV8304x EVM Sensored Software User's Guide* user's guide
- Texas Instruments, *BOOSTXL-DRV8304x EVM Sensorless Software User's Guide* user's guide
- Texas Instruments, *Brushless-DC Made Simple – Sensored Motor Control* TI TechNote
- Texas Instruments, *Field Oriented Control (FOC) Made Easy for Brushless DC (BLDC) Motors Using TI Smart Gate Drivers* TI TechNote
- Texas Instruments, *Hardware Design Considerations for an Efficient Vacuum Cleaner using BLDC Motor* application report
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle using BLDC Motor* application report
- Texas Instruments, *Industrial Motor Drive Solution Guide*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Motor Drive Protection With TI Smart Gate Drive* TI TechNote
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Reduce Motor Drive BOM and PCB Area with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Reducing EMI Radiated Emissions with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™ application report*
- Texas Instruments, *Understanding IDRIVE and TDRIVE In TI Motor Gate Drivers* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

NexFET, MSP430, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8304HRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8304H	Samples
DRV8304HRHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8304H	Samples
DRV8304SRHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8304S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

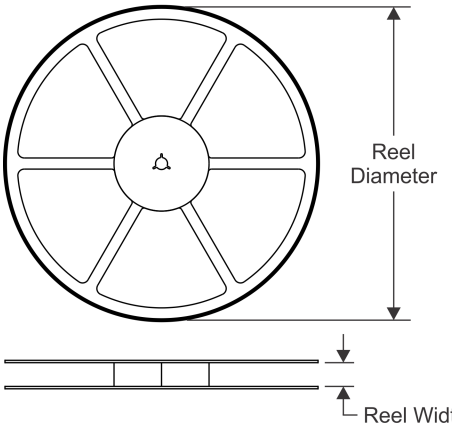
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

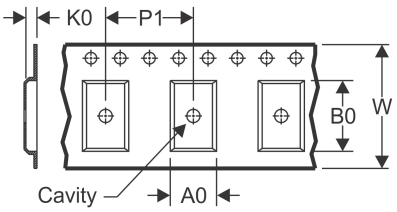
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

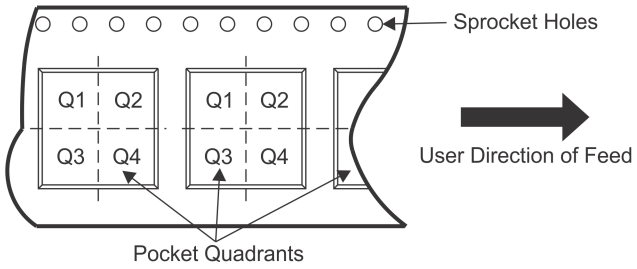


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

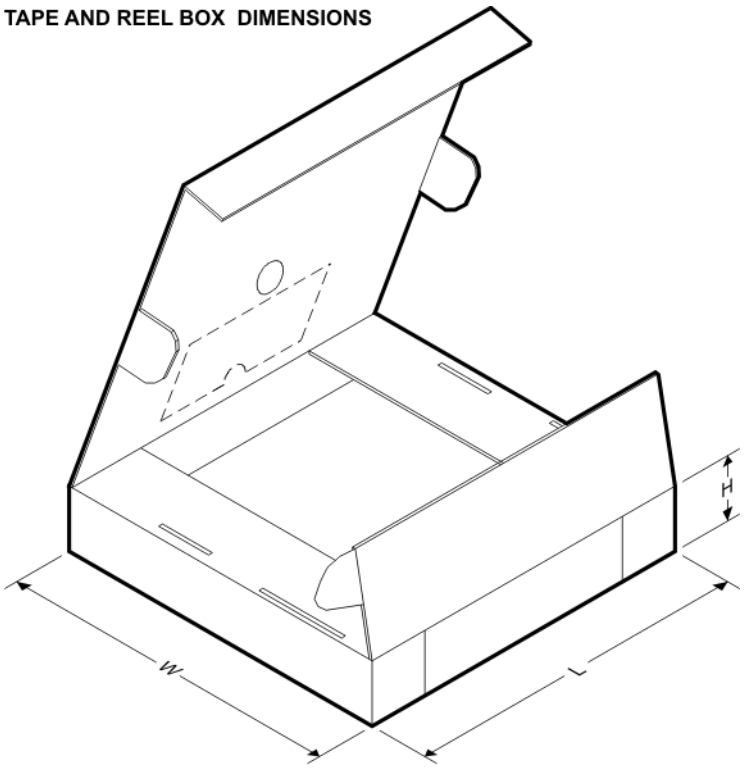
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8304HRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8304HRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8304SRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

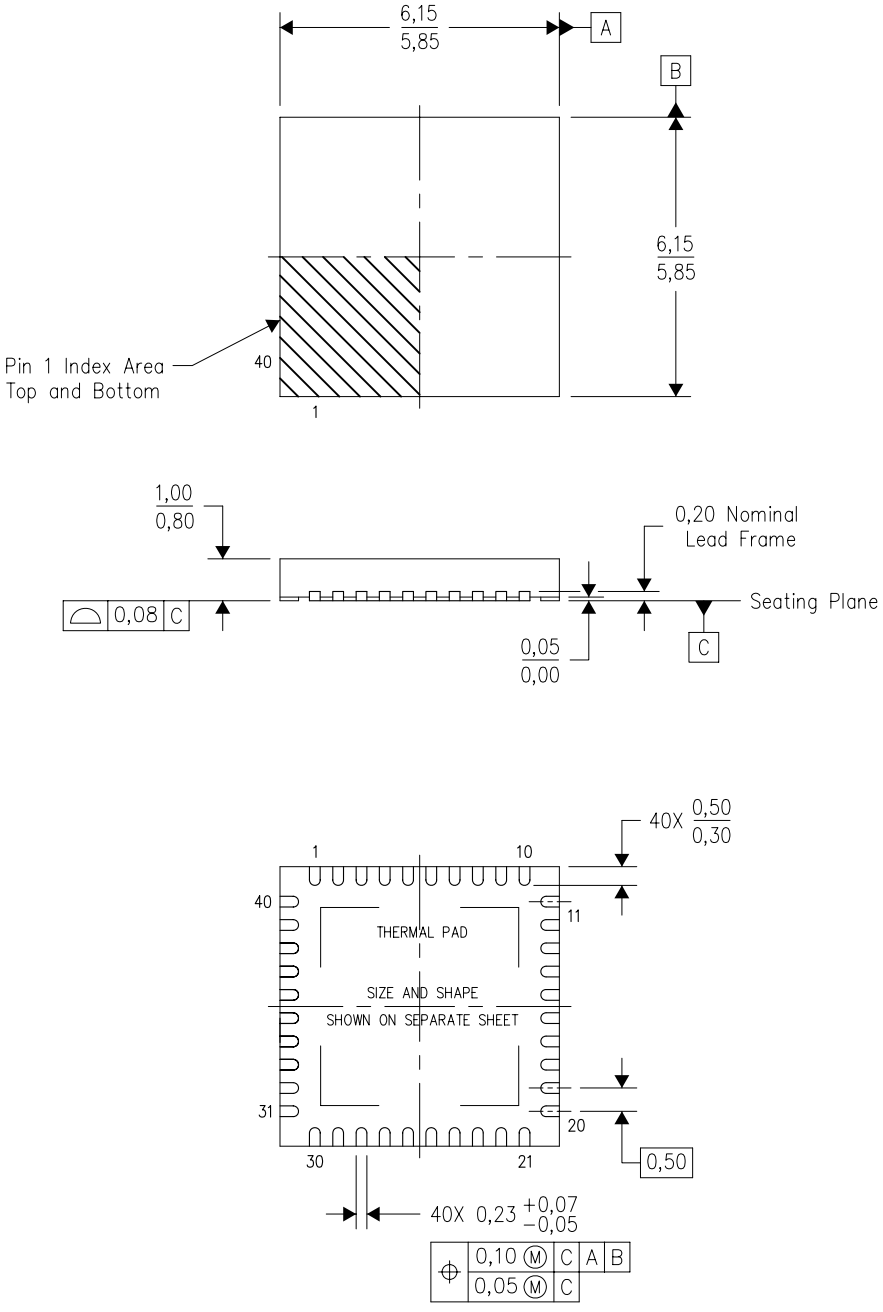
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8304HRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0
DRV8304HRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DRV8304SRHAR	VQFN	RHA	40	2500	367.0	367.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

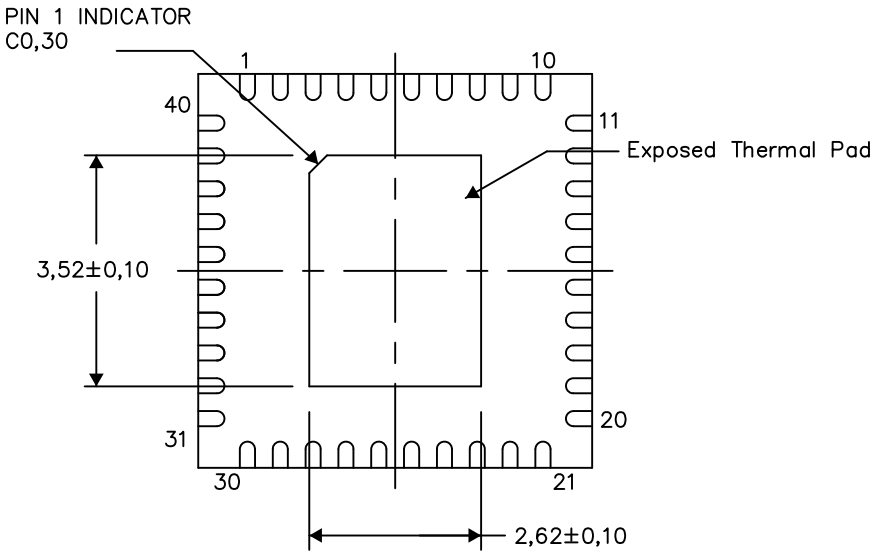
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



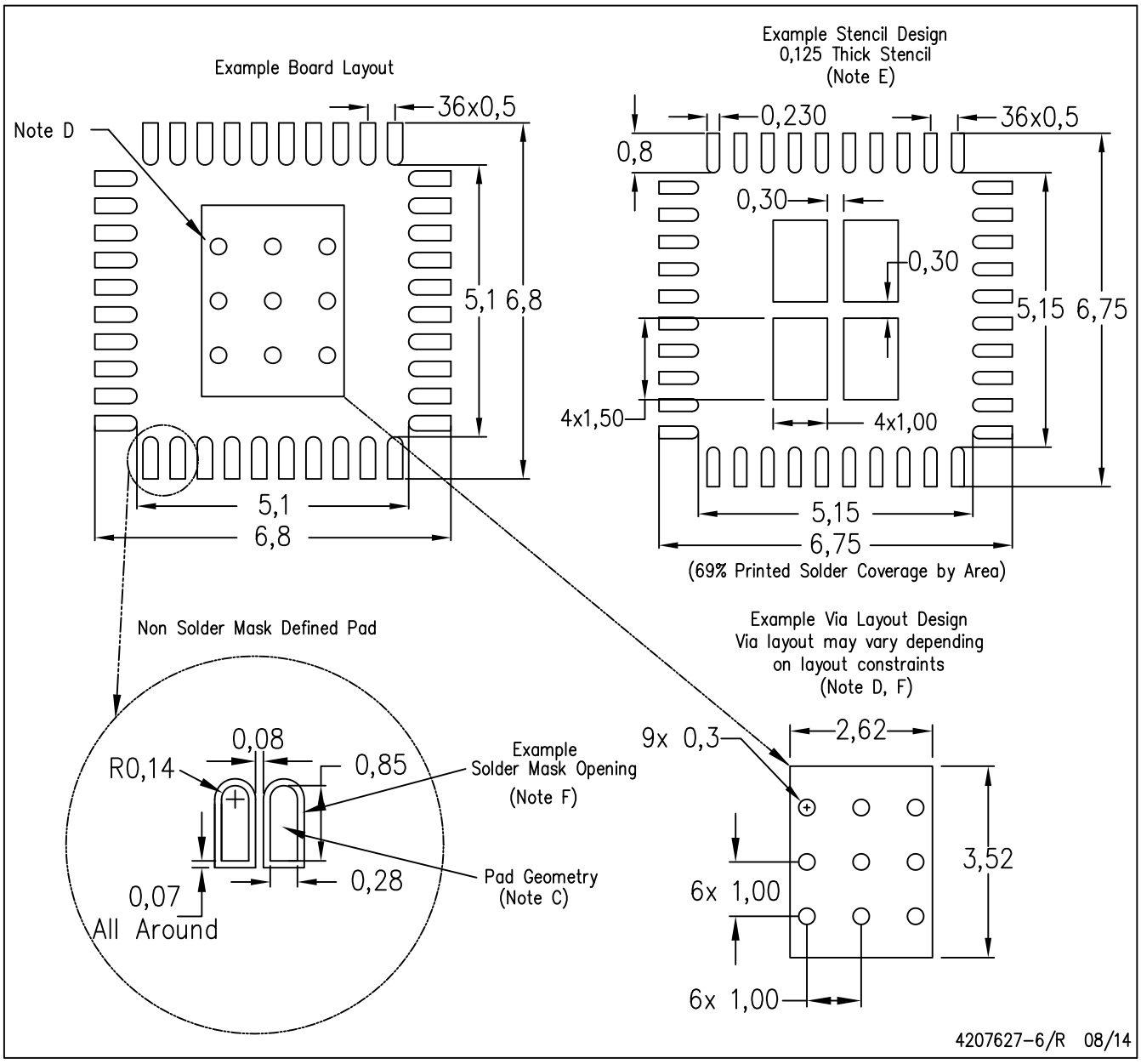
Bottom View

Exposed Thermal Pad Dimensions

4206355–9/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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