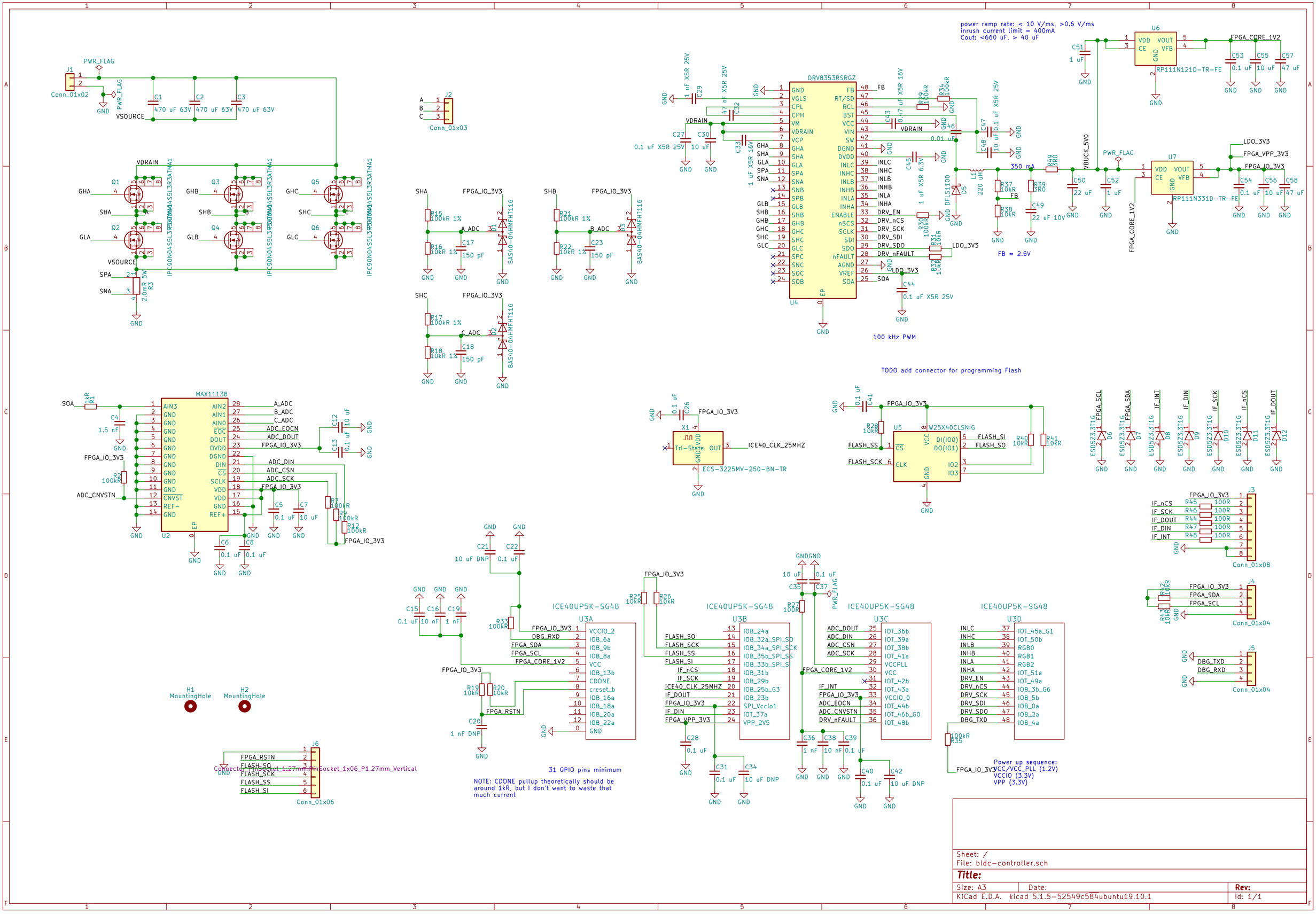
power ramp rate: < 10 V/ms, >0.6 V/ms
inrush current limit = 400mA
Cout: <660 uF, > 40 uF
DRV8353RSRGZ
U4
100 kHz PWM
FB = 2.5V
U6
RP111N121D-TR-FE
U7
RP111N331D-TR-FE
FPGA_CORE_1V2
FPGA_IO_3V3
LDO_3V3
FPGA_VPP_3V3
VBUCK_5V0
VSOURCE
VDRAIN
IPC90N04S5L3R3ATMA1
BAS40-04HMFHT116
MAX11138
U2
TODO add connector for programming Flash
U5
W25X40CLSNIG
ECS-3225MV-250-BN-TR
ESD5Z3.3T1G
Conn_01x08
Conn_01x04
Conn_01x06
Connector_FFCSocket_1.27mm_4PinSocket_1x06_P1.27mm_Vertical
ICE40UP5K-SG48
U3A
U3B
U3C
U3D
31 GPIO pins minimum
NOTE: CDONE pullup theoretically should be around 1kR, but I don't want to waste that much current
Power up sequence:
VCC/VCC_PLL (1.2V)
VCCIO (3.3V)
VPP (3.3V)
H1 MountingHole
H2 MountingHole
Sheet: /
File: bldc-controller.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 5.1.5-52549c584ubuntu19.10.1
Id: 1/1